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DIRECTORATE OF TECHNICAL EDUCATION
CHENNAI – 600 025

STATE PROJECT COORDINATION UNIT

Diploma in Electronics and Communication Engineering

Course Code: 1040

M – Scheme

e-TEXTBOOK
on
LINEAR INTEGRATED CIRCUITS
for
IV Semester DECE

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UNIT I

INTRODUCTION TO OPERATIONAL AMPLIFIERS

Integrated circuits –introduction:

The integrated circuit(IC) is ***a miniature, low cost electronic circuit*** **.**It has both ***active and passive components;*** they are joined together on a single crystal chip of silicon. When compared to conventional component the appearance of component in IC differs. But they perform similar electronic functions.

The components used to manufacture ICs are ***diode, transistor, MOSFET, resistors and capacitors.***

CLASSFICATION OF IC:

There are several ways of categorizing IC's.

1. **Depending upon the functional utility**
   - ❖ Linear ICs, and
   - ❖ Digital ICs

A linear (analog) IC performs ***amplification*** or other linear operation on signals. Hence it is also known as linear IC.

Digital IC performs the circuit function by dealing with discrete quantities. i.e., integer or fractional number. In digital IC, the information is represented by binary digits.

2. **Depending upon its structure**
   - ❖ Monolithic ICs
   - ❖ Thick film ICs
   - ❖ Thin film ICs
   - ❖ Hybrid ICs

In monolithic ICs, all the active and passive components along with their interconnections are manufactured on a single silicon chip.

The thick-thin ICs are used to produce only the passive elements. The thin film technology produces components with greater precision, but it is expensive as compared with the other technology.

Hybrid ICs are the combination of two or more monolithic ICs in one package. They may combine monolithic ICs with thick-thin film circuits.

3. Depending upon the active used

- ❖ Bipolar ICs
- ❖ Unipolar ICs

The bipolar ICs use ***bipolar junction transistors*** (BJTs), while the unipolar ICs use ***field effect transistors*** (FETs).

4. Depending upon the isolation technique used

The bipolar ICs are further classified as

- PN junction isolation ICs
- Dielectric ICs.

5. Depending upon the type of FET used

The unipolar ICs are further classified as

- MOSFET unipolar ICs
- JFET unipolar ICs.

ADVANTAGES OF IC OVER DISCRETE COMPONENTS

- ❖ Size of an IC is thousands of times smaller
- ❖ Thousands of silicon wafers consisting individually millions of components can be produced or manufactured simultaneously, known as mass production. Due to this, the cost of IC is very low.
- ❖ Weight of IC is very low.
- ❖ Power consumption of ICs is very low.
- ❖ Increased system reliability
- ❖ Matching of devices is excellent.
- ❖ Operating speeds are higher.

TYPES OF IC PACKAGES:

- ❖ First step to produce IC is the fabrication process. After completion of fabrication process several chips are ready on a single silicon wafer.
- ❖ Second step is to separate the individual chips. To do this,
    - Draw lines on a wafer using diamond tipped tool.
    - Then cut it along the lines.
- ❖ Finally, it is assembled on a suitable package.

The features of package depends upon

- ❖ Maximum pin count
- ❖ Dimensions
- ❖ Pitch (spacing between the centers of the adjacent pins)
- ❖ Encapsulating material (ceramic or plastic)
- ❖ Mode of mounting (plated through hole- TH or surface mount- SM)
- ❖ Maximum power dissipation.

TH (Through- Hole) mounting:

The standard packages are DIP (dual in the package) and PGA (Pin grid array)

Small scale integration (SSI) and medium scale integration (MSI) packages available in SIP (single in line package), ZIP (zigzag in line package) and QIPC (quad in line package) with TM mounting type.

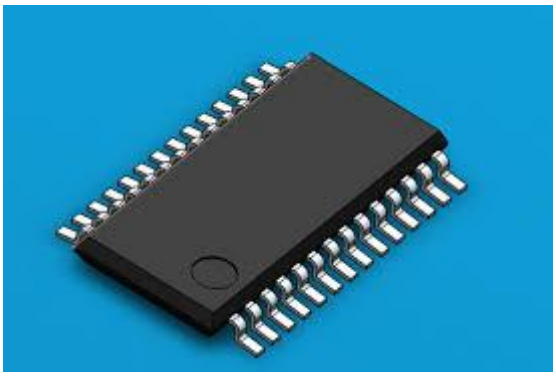
For low pin counts, SO (small outline package) and SSOP (shrunk small outline package) with SM (surface mount) mounting are available.

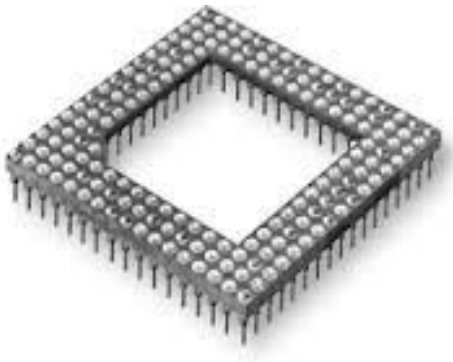
SM mounting types

- chip carrier (The chip carrier uses either plastic or ceramic.)
- TQFP (thin quad flat pack).

The different types of packages are shown in the given figure.

SOP **PGA**





SSOP **TQFP**

OPERATIONAL AMPLIFERS (IC741)

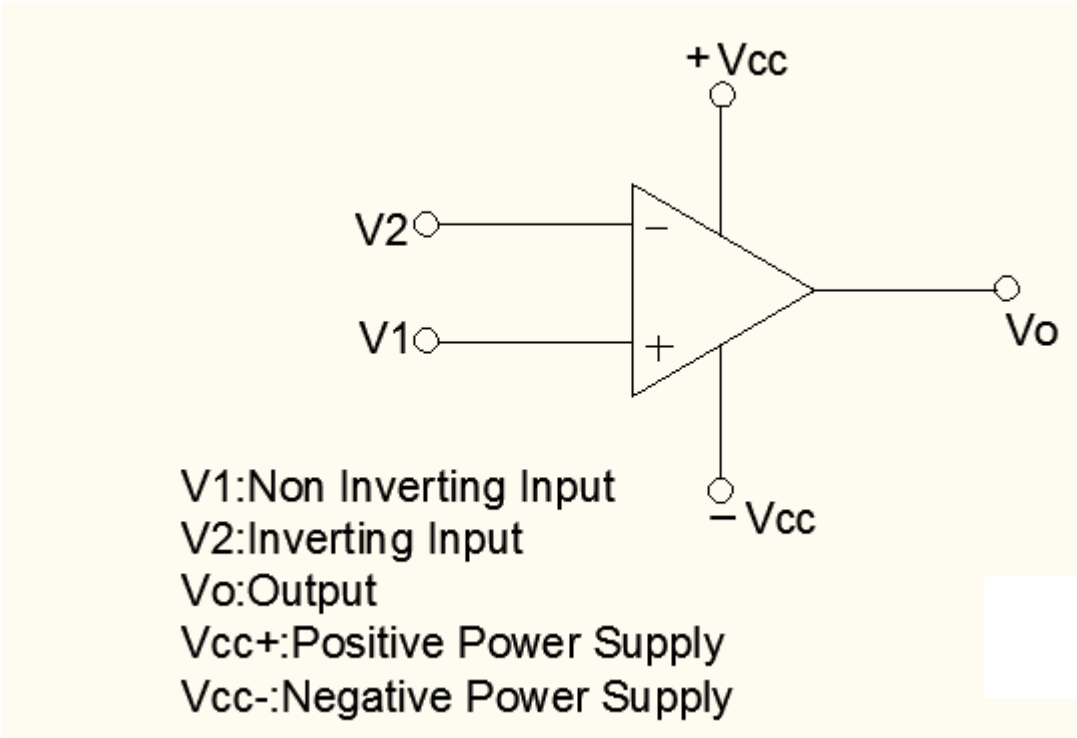
An operational amplifier is a ***direct coupled high gain negative feedback amplifier.*** It can amplify the signals in the range of***0Hz to 1MHz***. It is a basic linear integrated circuit.

In analog computers, it is designed to perform mathematics operations like addition, subtraction, differentiation, integration, multiplication, division etc., so, it is called as operational amplifier.

IC741 operational amplifier is an 8bit dual in line package IC. It is a very popular type IC. It has ***five basic terminals***.

- Two input terminals
- One output terminal
- Two supply terminals

SCHEMATIC SYMBOL FOR OP AMP:



It contains

⟶Two inputs

- Inverting input(V_1)
- non-inverting input (V_2)

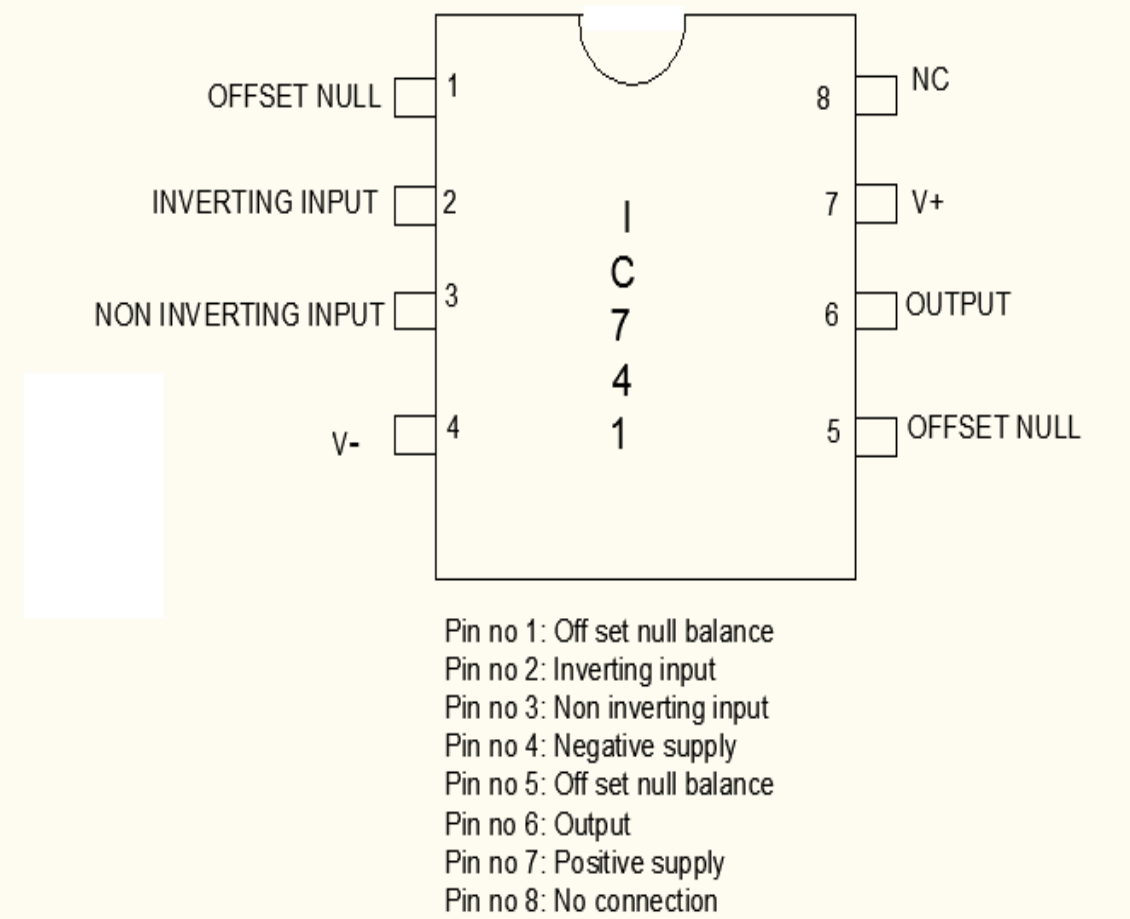
⟶ Only one output (V_o).

⟶A positive and a negative supply voltage are needed for its normal operation**.**

The signal given to the inverting input in always inverted at its output. A positive voltage at the inverting input produces a negative output voltage, and similarly a negative input voltage produces a positive output voltage. But the signal given to the non-inverting input will not produce any sign change at the output. The functions of an op-amp generally depends upon the external connected components.

PIN DIAGRAM OF OP-AMP IC 741

IC741 operational amplifier is an ***8 pin dual-in-line package IC***. The pin diagram of IC741 is shown in given figure.



Pin no 1: off-set null balance

Pin no 2: inverting input

Pin no 3: non-inverting input

Pin no 4: Negative supply

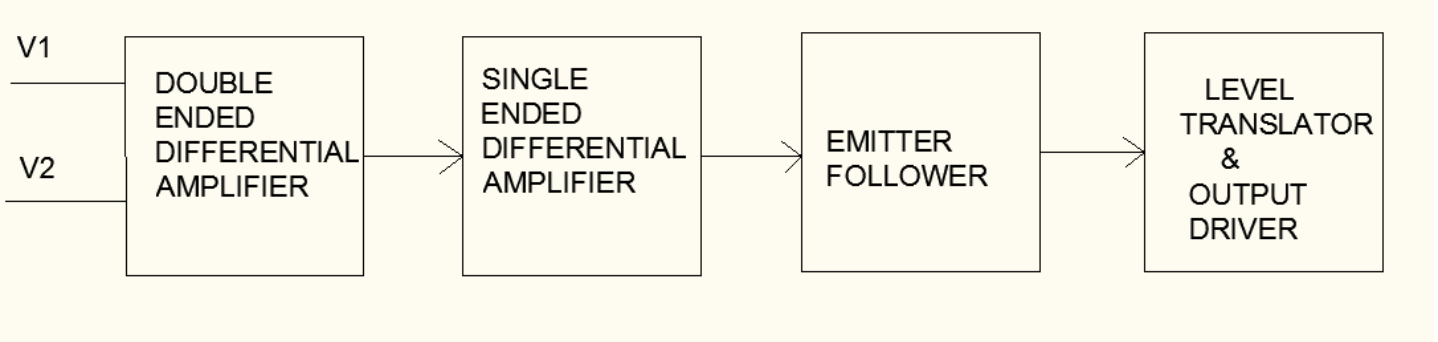
Pin no 5: off-set null balance

Pin no 6: output

Pin no 7: positive supply

Pin no 8: no connection

Block diagram of an OP-AMP:



An op-amp is a high quality amplifier.

It contains four stages

- Double ended differential amplifier
- Single ended differential amplifier
- Emitter follower
- Level transistor and output driver.

They are connected in cascaded manner.

Double ended differential amplifier:

This stage provides maximum voltage gain. This stage should employ a current source at the common emitter node for good common mode rejection.

Single ended differential amplifier:

It is also called as intermediate gain stage. It does not require a current source in the emitter. The purpose is to provide some additional gain. In order to prevent excessive loading of the first stage, its input resistance should be relatively high.

Level transistor and output driver

This stage is used to prevent undesired dc current in the load and increasing the permissible output voltage swing. Finally, it produces large output voltage or current.

CHARACTERISTICS OF AN IDEAL OP-AMP:

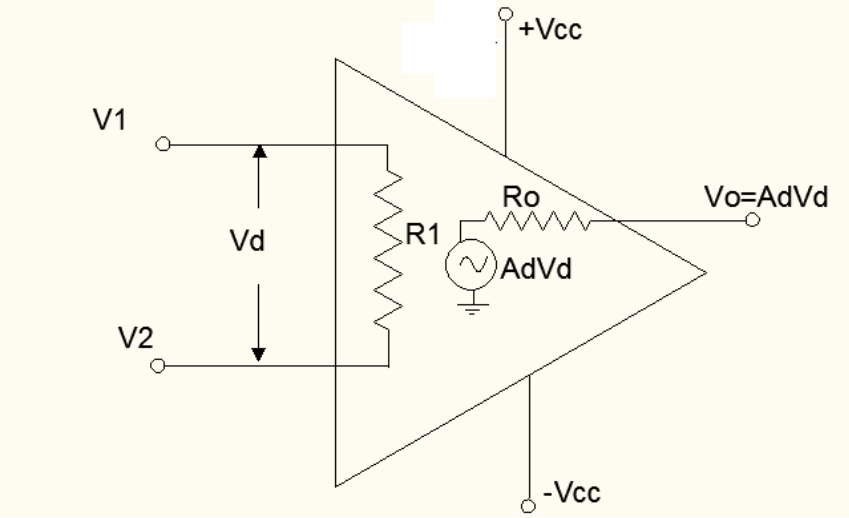
The ideal op-amp is a differential input, single ended output device. The characteristics are as follows.

- High input impedance, $R_i = \alpha$. (Practically 1 mega ohm)
- Low output impedance, $R_o = 0$ (Practically 1 to 2 ohm)
- High voltage gain, $A_V = \alpha$ (Practically several thousands)
- High bandwidth, BW = α (V restricted by slew rate)
- Perfect balance; V0 =0 when V1= V2.
- Characteristics do not drift with temperature.

Simple equivalent circuit of an op-amp:

The equivalent circuit is nothing but the representation of op-amp parameters in terms of its physical component. The equivalent circuit of an op-amp is shown in given figure.

Equivalent circuit of op-amp:



Here, the op-amp parameters the input resistance, output resistance, open loop voltage gain are represented in terms of circuit components like R_i, R_o etc. The op-amp amplifies the difference between the two input voltages.

$$\mathbf{V_o = A_d V_d = A_d (V_2 - V_1)}$$

Where, A_d = large signal open loop voltage gain
V_d = differential input voltage
V_1 = inverting input voltage with respect to ground
V_2 = non inverting input voltage with respect to ground

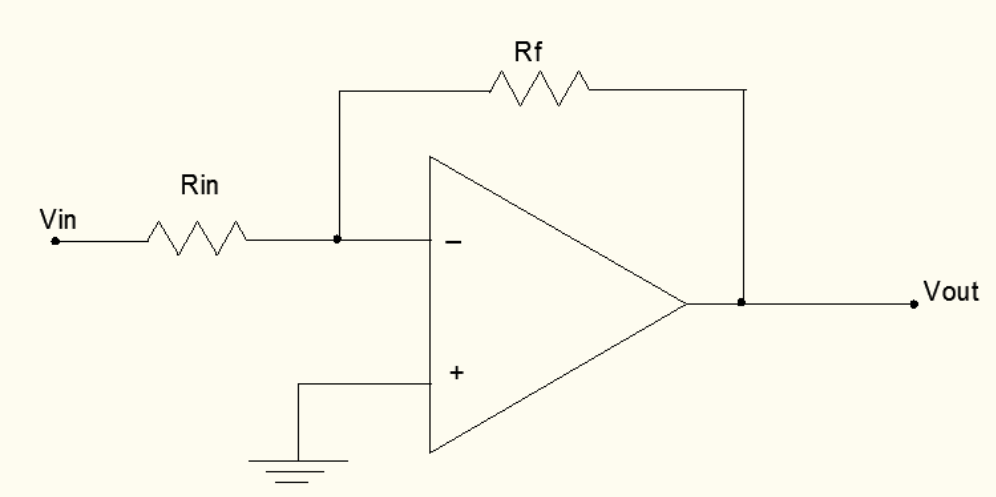
R_i = input resistance of op-amp
R_o = output resistance of op-amp

The output voltage is directly proportional to the difference voltage V_d. The op-amp amplifies the difference voltage and not the individual input voltages. Thus the polarity of output signal is decided by the polarity of the difference voltage V_d.

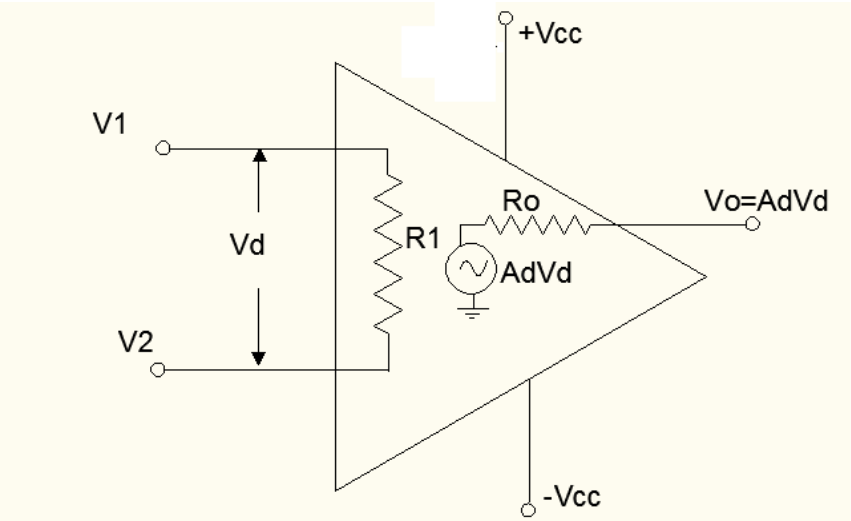
Application of op-amp

- Audio and video pre-amplifiers and buffers
- Voltage comparators
- Differential amplifiers
- Differentiators and integrators
- Filters
- Precision rectifiers
- Precision Peak Detector
- Voltage and current regulators
- Analogue calculators
- Voltage clamp
- Analog-to-digital converters
- Digital-to-analog converters

VIRTUAL GROUND:



An inverting amplifier is shown in above figure. In this figure, non-inverting input is grounded, and the input signal (V_i) is applied to the inverting input terminal through a resistor R_i.



The figure represents equivalent circuit of op-amp.

In general the output voltage of an op-amp

$$V_o = A_d V_d = A_d (V_2 - V_1)$$

A_d = large signal open loop voltage gain
V_d = differential input voltage
V_1 = inverting input voltage with respect to ground
V_2 = non- inverting input voltage with respect to ground

Assuming $V_o = V_2 - V_1$

$$V_d = V_o/A_d$$

Since Ad is very large, $V_d = 0$

$$V_1 \cong V_2$$

The voltage at the inverting terminal (V_1) is approximately equal to that at the non-inverting terminal (V_2).So, the differential voltage is zero. In other words, the inverting terminal voltage Vs is approximately at ground potential because V_2 is directly connected to ground. That means, the inverting terminal is not directly connected to ground, but it acts like a ground terminal. Therefore the inverting terminal is said to be at virtual ground.

PARAMETERS OF OP-AMP:

Input offset voltage:

It is the input voltage which should be applied between the input terminals to get zero output voltage.

Input offset current:

It is the difference between the currents entering the inverting and non-inverting input terminals of an operational amplifier.

Input bias current:

It is the average of the currents that enter into the inverting and non-inverting input terminals of a operational amplifier.

Output offset voltage:

It is the output voltage present, when the two input terminals are grounded.

Differential input resistance:

It is the equivalent resistance that can be calculated at either the inverting or non-inverting input terminal with the other terminal connected to ground.

Input capacitance:

It is the equivalent capacitance that can be calculated at either the inverting or non-inverting terminal with the other terminal connected to ground.

Open loop voltage gain (Av):

When the op-amp is used without any feedback, the differential voltage gain is known as open loop voltage gain.

Supply voltage rejection ratio (SVRR):

It occurs because of supply voltage variations, which leads to changes in input offset voltage.

SVRR is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power voltages held constant.

Output voltage swing:

It is the maximum peak-to-peak output voltage (+ve or –ve saturation voltage) which can be obtained without waveform clipping when DC output is zero.

Slew rate (SR):

It is defined as the maximum rate of change of output voltage per unit of time. It is expressed in volts per microseconds.

$$\mathbf{SR} = \frac{\mathbf{dV_0}}{\mathbf{dt}} \mathbf{/maximum}$$

Common mode rejection ratio (CMRR)

CMRR is the ratio of differential voltage gain (A_d) to the common mode voltage gain (A_{cm}).

$$\mathbf{CMRR} = \frac{\mathbf{A_d}}{\mathbf{A_{cm}}}$$

Maximum differential input voltage:

It is the maximum value of differential input voltage that can be applied without damaging the op-amp.

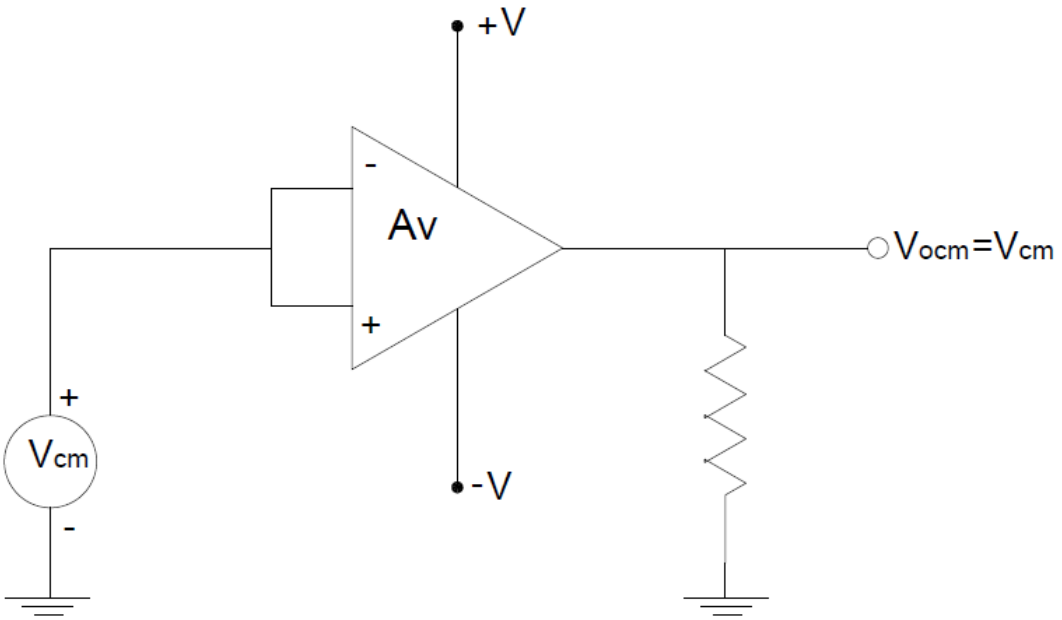
Maximum common mode input voltage:

It is the maximum voltage to which that the two inputs can be raised above ground potential before the op-amp.

COMMON MODE REJECTION RATIO (CMRR)

A***n op-amp is said to be operating in common mode configuration when the same input voltage is applied to both the input terminals.***

CMRR is the ratio of differential voltage gain (A_d) to common mode voltage gain (A_{cm}).



Since the input voltage applied is common to both inputs, it is referred to as common mode voltage V_{cm}. A common mode voltage can be AC, DC or combination of both AC and DC.

Ideally an op-amp amplifies only differential input voltage. So, there is no common mode output voltage (V_{ocm}) at the output. Due to the imperfections of op-amp, some common mode voltage V_{ocm} will appear at the output. The amplitude of this V_{ocm} is very small and often insignificant compared to V_{cm}.

Therefore an op-amp amplifies only differential input voltage. Ratio of common mode output voltage (V_{ocm}) to the input common mode voltage (V_{cm}) is called common mode voltage gain (A_{cm}). It is generally much smaller than 1.

In general, $\mathbf{CMRR} = \frac{\mathbf{A_d}}{\mathbf{A_{cm}}}$

The CMRR can also be expressed as the ratio of the change in input offset voltage (V_{io}) to the total change in common mode voltage (V_{cm}).

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

The value of CMRR is very large; therefore it is usually specified in decibels (dB)

$$\text{CMRR in dB} = 20\log \frac{A_d}{A_{cm}}$$

Or

$$\text{CMRR in dB} = 20\log \frac{V_{io}}{V_{cm}}$$

Practically, op-amps with higher CMRR are used. Because, it has the ability to reject common mode voltages. The CMRR is a function of frequency and decreases as the frequency is increased.

SLEW RATE:

Slew rate is an important frequency related parameter of an op-amp. ***It is the maximum rate of change of output voltage with respect to time, usually specified in V/μs.***

For example a 1 V/μs slew rate means that the output changes (may be rise or fall)no faster than 1V per microsecond. The slew rate improves with higher closed loop gains and dc supply voltages.

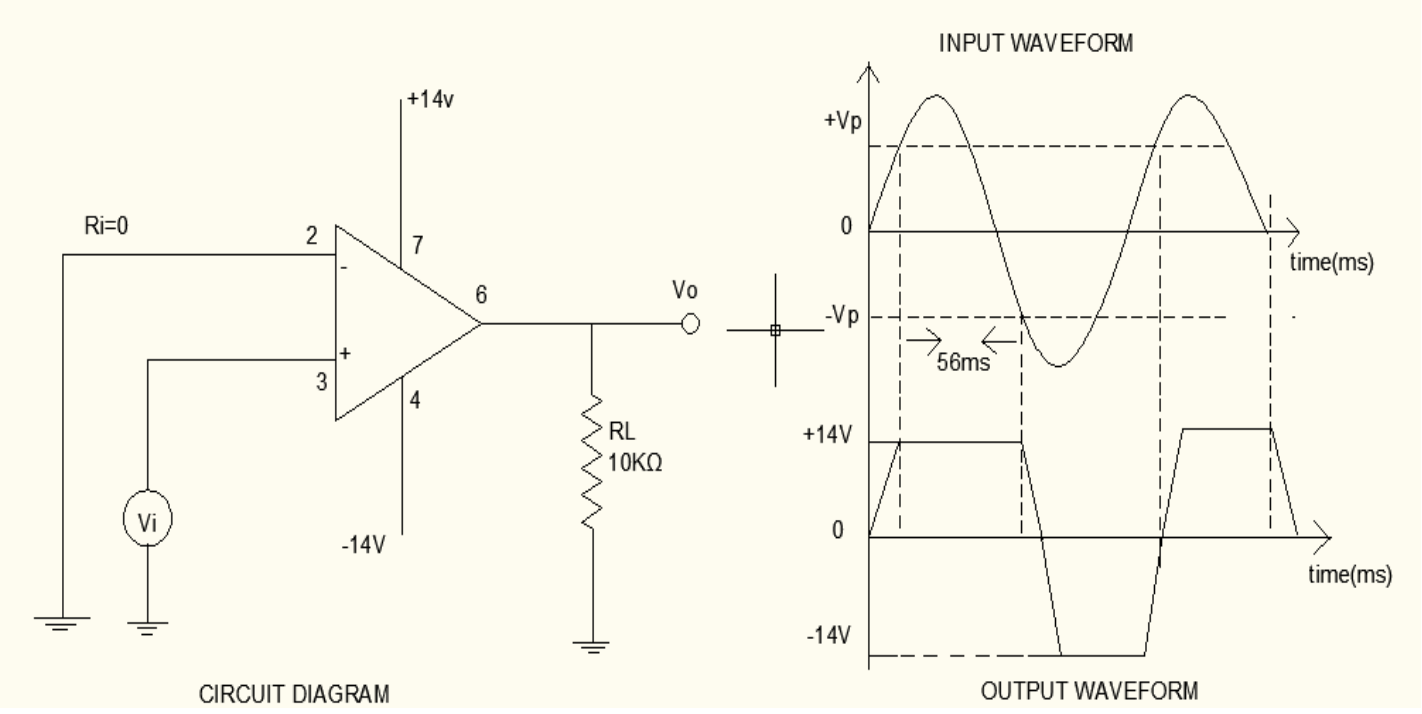
Ideally slew rate is infinite. Because, op-amp produces immediate change in output (oscillations) with fast changing input. It can be avoided by using a capacitor within or outside the op-amp.

Slew rate, $\mathbf{SR} = \frac{\mathbf{2\pi F V_P}}{\mathbf{10^4}} \mathbf{V/\mu}$

Where, F = input frequency (Hz)
V_p = peak value of the output sine wave (Volts)

If either the frequency or amplitude of the input signal is increased to exceed the slew rate of op-amp, the output will distort.

The slew rate has important effects on both open loop and closed loop op-amp circuits. The open loop configuration using op-amp IC 741 is shown in the given figure. Since the open loop voltage gain is very large, the output will go to about +14V and then to -14V each time the input sine wave crosses zero volts, as shown in given figure.



The time taken by the output to go form +14V to -14V can be determined by using the slew rate of the IC 741 listed in the data sheet.

The IC 741 has a typical slew rate of 0.5V/μs

Therefore $\frac{28V}{0.5V/\mu s} = 56\mu s$
(28V is the difference between +14V and -14V)
It must be minimum time between the two zero crossings. Hence at the maximum input frequency f_{max} at which the output will be distorted is given by

$$F_{max} = \frac{1}{(2)(59\mu s)} = 8.93kHz$$

Thus to have a more square wave output either we keep the input frequency below F_{max} or choose an op-amp with a faster slew rate.

BASIC LINEAR CIRCUITS:

Generally operational amplifiers are used for negative feedback.

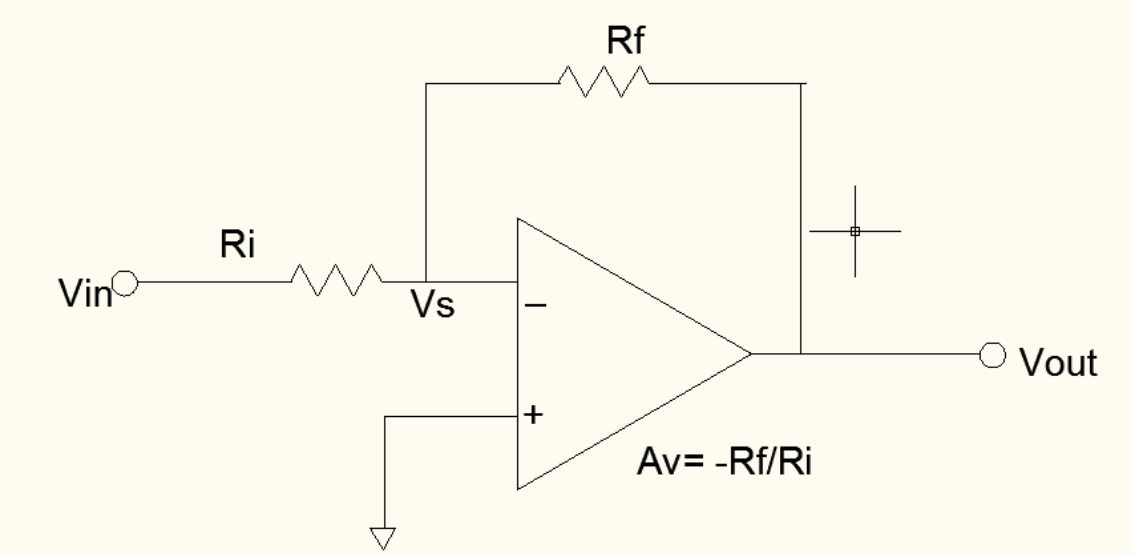
Operational amplifier using IC's is inexpensive, versatile and easy to use.

For this reason they are also used for wave shaping, filtering and mathematical operations. Some commonly used applications are discussed below.

OP-AMP AS INVERTING AMPLIFIER:
DEFINITION:
If a signal (ac or dc) is applied to the inverting input terminal and –ve feedback is given, then the circuit amplifies by inverting the input. Such a circuit is called inverting amplifier.

WORKING:

The given figure shows an inverting amplifier using op-amp.



From the circuit, when a voltage V_i is applied to its input, the current i_1 is flowing through R_i (input resistor), and also the current if is flowing through R_f (feedback resistor). Since its input impedance is high, no current enters into an operational amplifier.

i_1 – Current flows through R_i

i_f – Current flows through R_f

V_s – Ground potential

Applying Kirchhoff's current law at the inverting node,

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_o}{R_f}$$

Vs = 0, because it is virtual ground.

Hence $\frac{V_i}{R_i} = -\frac{V_0}{R_f}$

$$V_0 = -\frac{R_f}{R_i} \times V_i$$

$$= \frac{R_f}{R_i} \times (-V_i)$$

$$\text{Voltage gain, } A_v = \frac{V_0}{V_i} = -\frac{R_f}{R_i}$$

The input voltage is amplified in accordance with the values (ratio) of R_f and R_i, and also inverted.

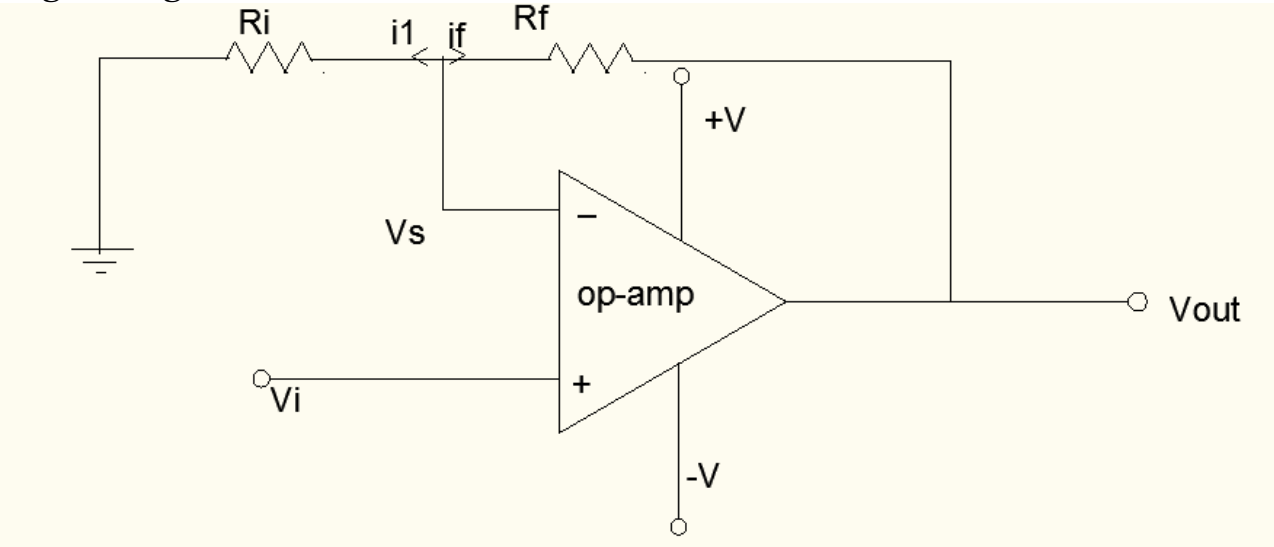
OP-AMP AS NON-INVERTING AMPLIFIER:

DEFINITION:

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given, then ***the circuit amplifies without inverting the input***. Such a circuit is called non-inverting amplifier.

WORKING:

The circuit diagram of non-inverting amplifier using op-amp is shown in given figure.



The input voltage V_i is directly applied to the non-inverting terminal. According the characteristics of an op-amp, the applied input voltage V_i is also developed at the inverting input terminal (V_s).

$$V_s = V_i$$

Applying Kirchhoff's current law

$$i_1 = i_f$$

$$\frac{V_s}{R_i} = \frac{V_0 - V_s}{R_f}$$

$$\frac{V_i}{R_i} = \frac{V_0 - V_i}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_i}{R_i} + \frac{V_i}{R_f}$$

$$\frac{V_0}{R_f} = V_i\left(\frac{1}{R_i} + \frac{1}{R_f}\right) = \left(\frac{R_i + R_f}{R_f R_i}\right) V_i$$

$$V_0 = \cancel{R_f}\left(\frac{R_i + R_f}{\cancel{R_f} R_i}\right) V_i$$

$$V_0 = \left(\frac{\cancel{R_i}}{\cancel{R_i}} + \frac{R_f}{R_i}\right) V_i$$

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_i$$

$$\text{Voltage gain, } A_v = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_i}$$

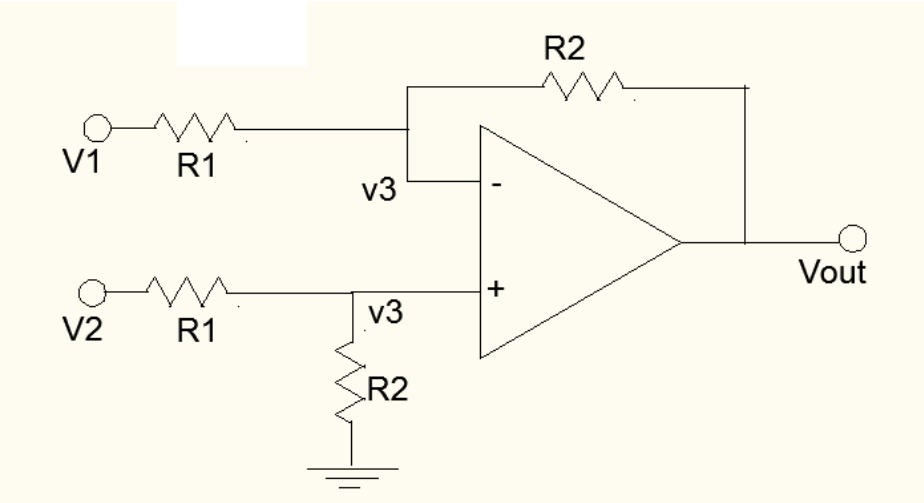
The output voltage is always in phase with the input. The gain of this amplifier also depends upon the external connected components of R_f and R_i.

Difference between Inverting Amplifier and Non-inverting Amplifier:

Inverting Amplifier	**Non-inverting Amplifier:**
The input is given to the inverting input terminal of the op-amp.	The input is given to the non-inverting input terminal of the op-amp.
It gives an inverted output.	It gives an output which is in phase with the input signal.
The gain of the inverting amplifier, when used with a negative feedback, is directly proportional to the ratio of the feedback resistor/ input resistor.	The gain of the non-inverting amplifier is also proportional to the ratio of the feedback resistor/ input resistor but with an intercept value.

OP-AMP AS DIFFERENTIAL AMPLIFIER:

Differential amplifier will amplify the difference between the two input signals.



The circuit diagram of differential amplifier is shown in above figure. Since the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at same potential, assumed as V_3.

The nodal equation at 'a' is

$$i_1 = i_2$$

$$\frac{V_1 - V_3}{R_1} = \frac{V_3 - V_o}{R_2}$$

$$\frac{V_1}{R_1} - \frac{V_3}{R_1} - \frac{V_3}{R_2} = -\frac{V_0}{R_2}$$

$$\frac{V_1}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = -\frac{V_0}{R_2} \ldots\ldots\ldots\ldots (1)$$

The nodal equation at 'b' is

$$i_3 = i_4$$

$$\frac{V_2 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\frac{V_2}{R_1} - \frac{V_3}{R_1} - \frac{V_3}{R_2} = 0$$

$$\frac{V_2}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = 0 \ldots\ldots\ldots\ldots (2)$$

Subtracting equ (1) from equ (2)

$$\frac{V_2}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = 0 \ldots\ldots\ldots\ldots (2)$$

(-)

$$\frac{V_1}{R_1} - V_3\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = -\frac{V_0}{R_2} \ldots\ldots\ldots\ldots (1)$$

(-) (+) (+)

$$\frac{V_2}{R_1} - \frac{V_1}{R_1} = 0 + \frac{V_0}{R_2}$$

$$\frac{V_2}{R_1} - \frac{V_1}{R_1} = \frac{V_0}{R_2}$$

$$\frac{V_2 - V_1}{R_1} = \frac{V_o}{R_2}$$

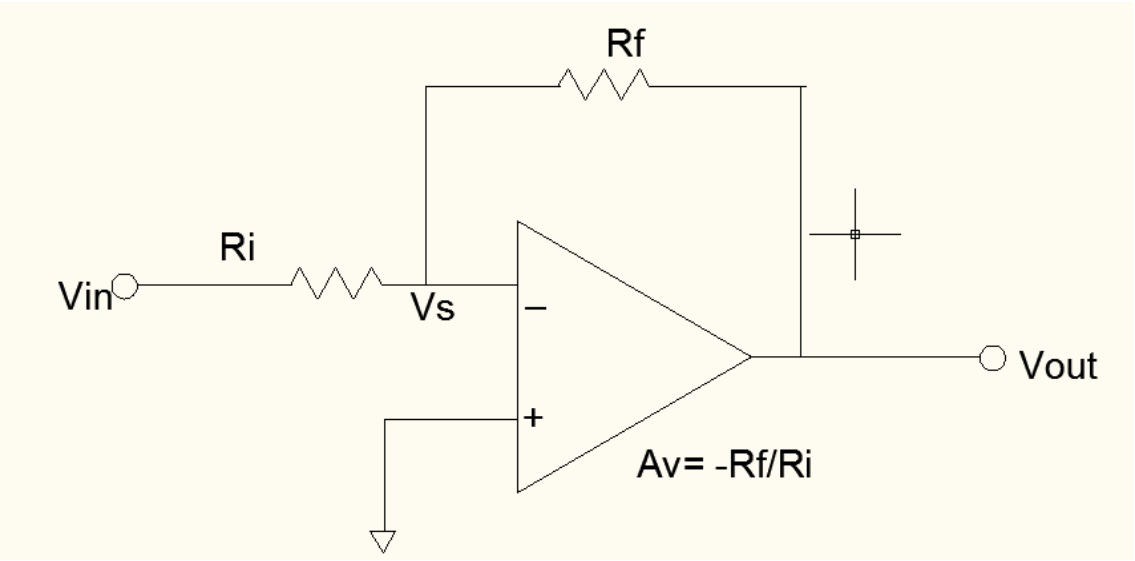
$$V_0 = \frac{R_2}{R_1}(V_2 - V_1)$$

$$V_0 = A_v(V_2 - V_1)\left(\therefore A_v = \frac{R_2}{R_1}\right)$$

If can be considered as instrumentation amplifier. But it is not used as an instrumentation amplifier because imbalance may be produced by circuit components.

SIGN CHANGER:

A circuit which produces an output signal with the same magnitude of the input signal but out of phase is called sign changer.



It is a basic inverting amplifier.

The output of inverting amplifier,

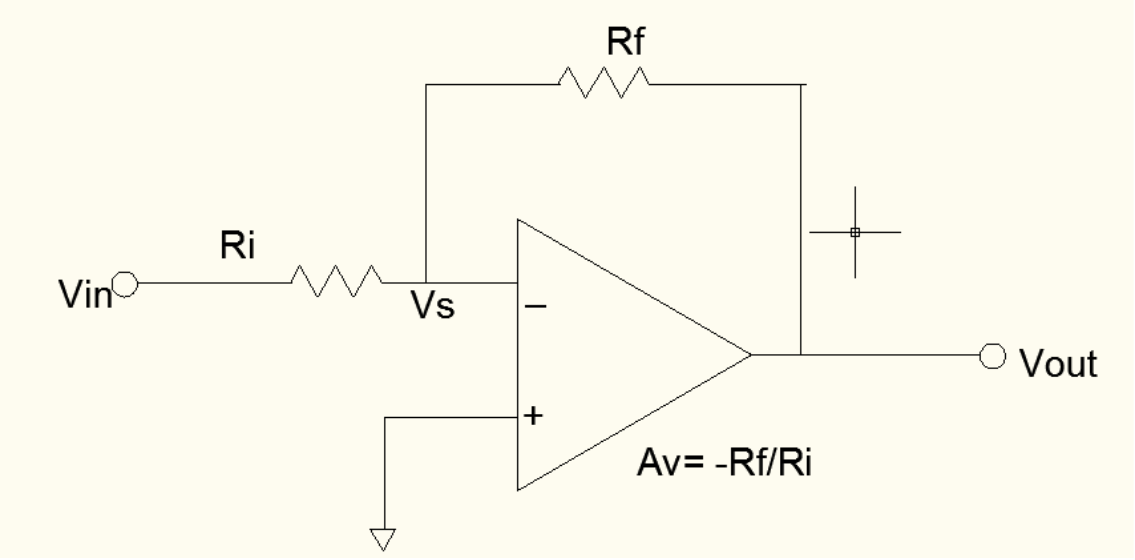
$$V_0 = -\frac{R_f}{R_i} \times V_i$$

Choose $R_f = R_i$

Then, it becomes $V_0 = -V_i$

Now the circuit will operate as sign changer.

SCALE CHANGER:



It is a basic inverting amplifier.

The output of inverting amplifier,

$$V_0 = -\frac{R_f}{R_i} \times V_i$$

Choose $R_f = KR_i$

Then $\frac{R_f}{R_i} = k$

$$V_0 = -K \times V_i$$

Thus the output is k times of the input signal, and it has 180 ° phase shift with input.

UNIT II

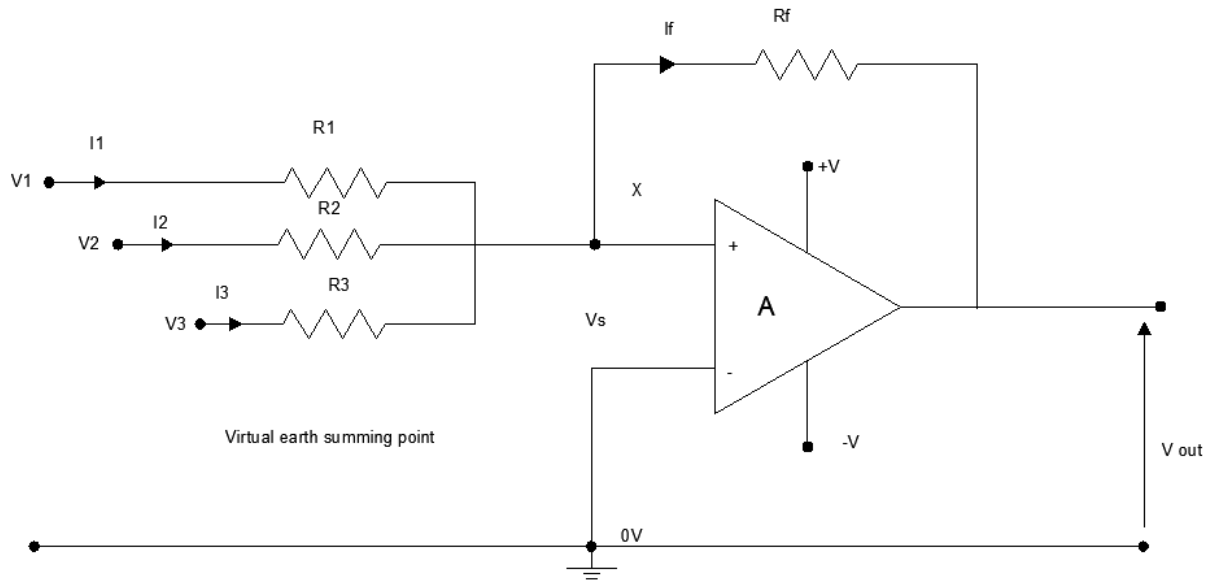
OP AMP - APPLICATIONS

APPLICATIONS OF OP-AMP:

Operational amplifier using IC is inexpensive, versatile and easy to use. For these reasons, they are used not only for negative feedback amplifies but also used for wave shaping, filtering and mathematical operations. Some commonly used applications are discussed below.

Adder:

The amount of voltage produced at the output of adder is equal to the algebraic sum of input signal voltages.



An adder is an arithmetic circuit. A typical three input adder circuit is shown in above figure. The input voltages are applied to the inverting input through separate input resistors R_1, R_2 and R_3.

According to Kirchhoff's current law at the inverting terminal,

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_1 - V_s}{R_1} + \frac{V_2 - V_s}{R_2} + \frac{V_2 - V_s}{R_3} = \frac{V_s - V_0}{R_f}$$

$$\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}=-\frac{V_0}{R_f}\ (\text{since } V_S=0)$$

ASSUME: $R_1=R_2=R_3=R_f=R$

$$\frac{V_1}{R}+\frac{V_2}{R}+\frac{V_3}{R}=-\frac{V_0}{R}$$

Now, commonly take $\frac{1}{R}$ outside.

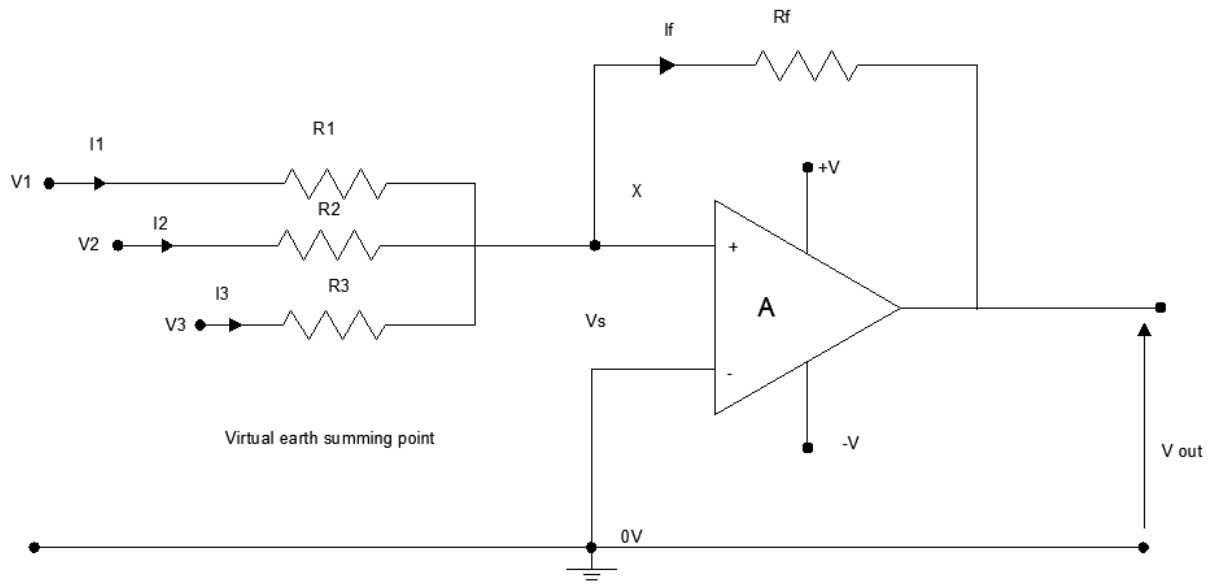
$$\frac{1}{R}(v1+v2+v3)=-\frac{v_0}{R}$$

$$V_0=-(V_1+V_2+V_3)$$

From this, we can understand the output voltage V_o is the sum of input signal voltages called adder.

SUMMING AMPLIFIER:

A typical three input summing amplifier is shown in given figure. It is also identical with the circuit of an added.



According to the Kirchhoff's current law at the inverting terminal,

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f} \text{ (since } V_s = 0)$$

Choose: $R_1 = R_2 = R_3 = R$, the above equation becomes

$$\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} = -\frac{V_0}{R_f}$$

Now, commonly take $\frac{1}{R}$ outside.

$$\frac{1}{R}(V_1 + V_2 + V_3) = -\frac{V_0}{R_f}$$

$$V_0 = -\frac{R_f}{R}(V_1 + V_2 + V_3)$$

Assume, $A_v = -\frac{R_f}{R}$

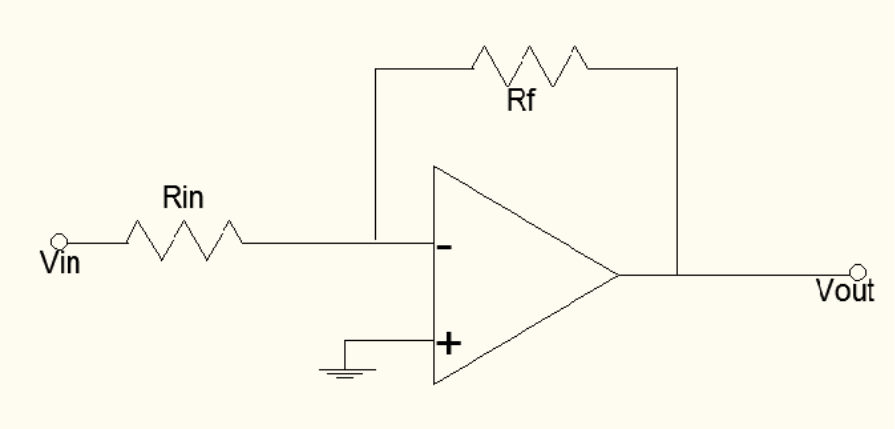
$$V_0 = A_v(V_1 + V_2 + V_3),$$

The output signal is the amplification of sum of input signal voltages.

MULTIPLIER:

A multiplier multiple the input voltage to a particular amount.

Multiplier is the application of inverting amplifier. The circuit diagram of multiplier is shown in given figure.



By using the Kirchhoff's current law,

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_0}{R_f}$$

$V_s = 0$, it is virtual ground.

$$\frac{V_i}{R_i} = \frac{-V_0}{R_f}$$

$$-V_0 = \frac{V_i}{R_i} R_f$$

$$V_0 = \frac{-V_i}{R_i} R_f$$

$$V_0 = -\frac{R_f}{R_i} V_i$$

The multiplication factor, $M = \frac{R_f}{R_i}$

Hence $V_o = -M\ V_i$

Now we can understand that the multiplication factor depends upon the ratio of R_f and R_i.

The output voltage is M times multiplication of input voltage. For multiplication the value of R_f should be higher than R_i.

If R_f = 10kΩ and Ri = 1kΩ, the multiplication factor

$$M = \frac{10k\Omega}{1k\Omega} = 10$$

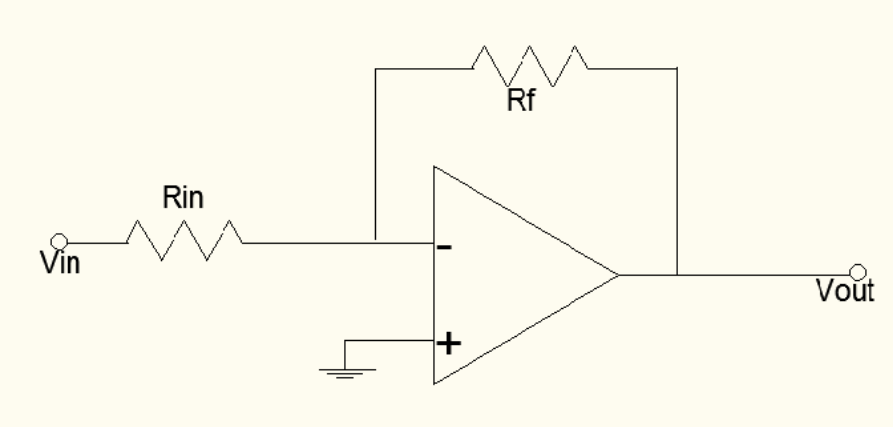
Now $V_o = -10V_i$

The input voltage multiplies with the factor of 10.

DIVIDER:

A divider divides the input voltage to a particular amount.

Divider is also the application of inverting amplifier. The circuit diagram of divider is shown in given figure.



By using Kirchhoff's current law

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_0}{R_f}$$

$V_s = 0$, it is virtual ground.

$$\frac{V_i}{R_i} = \frac{-V_0}{R_f}$$

$$-V_0 = \frac{R_f}{R_i} V_i$$

$$V_0 = -\frac{R_f}{R_i} V_i$$

The divider factor, $D = \frac{R_i}{R_f}$

$$\frac{R_f}{R_i} = \frac{1}{D}$$

Hence $V_0 = -\frac{V_i}{D}$

For divider operation, the value of R_i should be higher than R_f.

The output voltage is D times division of input voltage.

If R_i = 10kΩ and R_f = 1kΩ, the dividend factor

$$D = \frac{10k\Omega}{1k\Omega} = 10$$

The output voltage, $V_0 = -\frac{V_i}{10}$

The input voltage divides with the factor of 10.

VOLTAGE FOLLOWER:

The output voltage follows the input voltage.

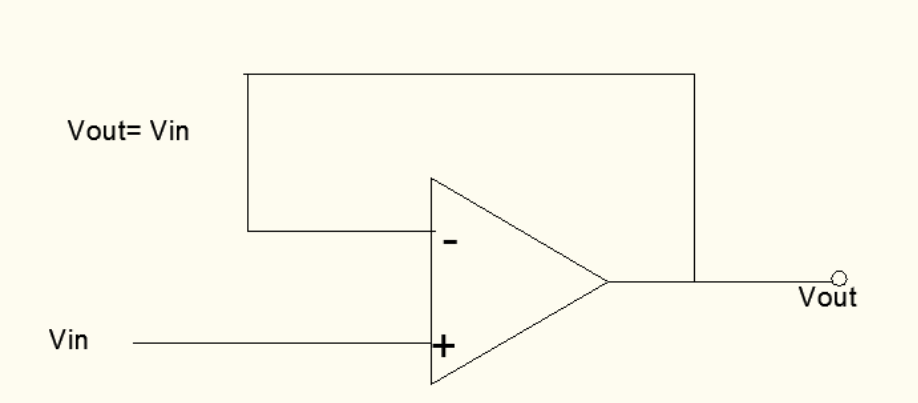
In a non-inverting amplifier, the output voltage is given by,

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_i$$

When R_f = 0 and R_i = α, the output voltage becomes

$$V_0 = (1 + 0)V_i$$

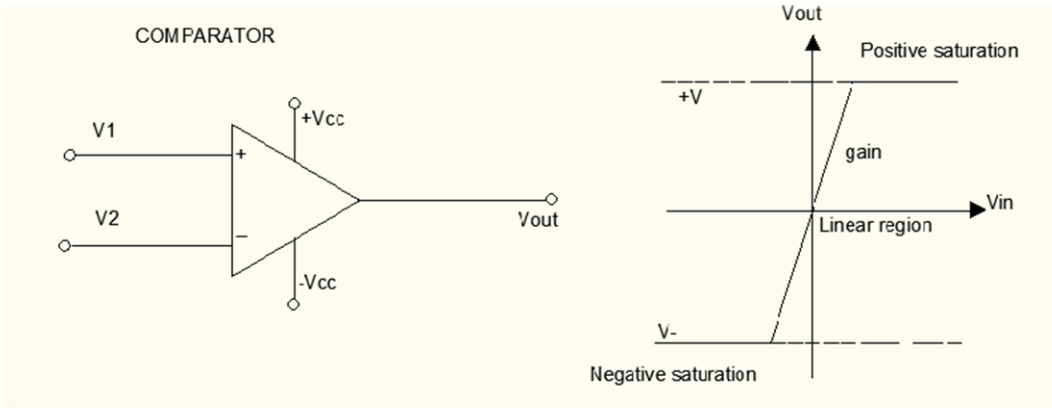
$$V_0 = V_i$$



The modified circuit shown in the above figure is called voltage follower. The voltage follower is also called ***unity gain amplifier***.

COMPARATOR:

The circuit diagram and response characteristics of comparator are shown in given figure. It contains two input terminals and only one output terminal. The voltage applied to the inverting input is V_1 and the non-inverting input is V_2.

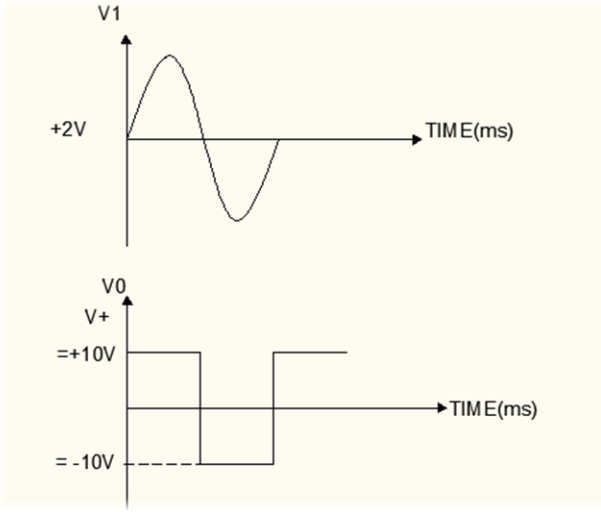


When V_1 is greater than V_2, the input differential voltage($V_2 - V_1$) is negative then the output reaches maximum negative, typically equal or less than the negative supply voltage (negative saturation). Similarly, when V_2 is greater than V_1 the input differential voltage($V_2 - V_1$) is positive and the output reaches maximum positive, typically equal to or less than the positive supply voltage (positive saturation). When V_1 is equal to V_2, output goes to zero.

It is summarized as follows

(i) **When V_1 (-) > V_2 (+); V_o = - V_{sat}**
(ii) **When V_2 (+) > V_1 (-); V_o = +V_{sat}**
(iii) **When V_1 (-) = V_2 (+); V_o = 0 volt**

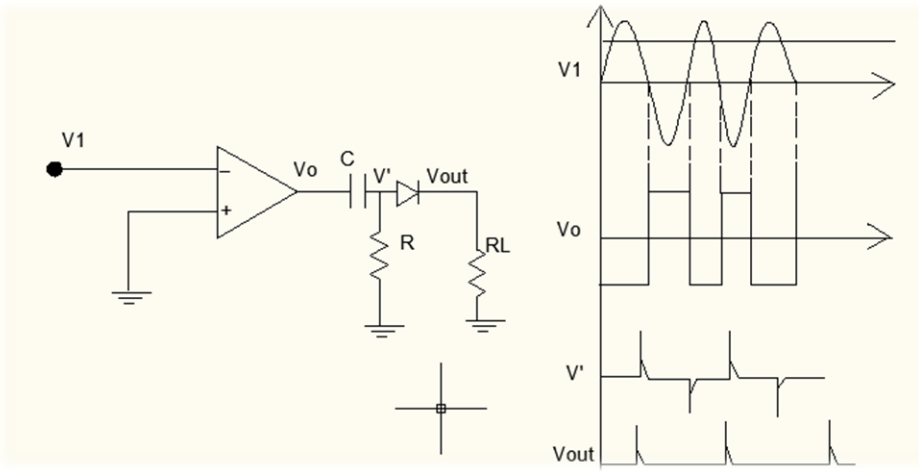
One application of comparator for converting a sine wave signal into a square wave signal is shown in the given figure.



- During positive half cycles of input, the non-inverting input voltage is higher than the inverting input voltage. So, the output goes to +ve saturation level($+V_{sat}$)
- During negative half cycles of input, the non-inverting input voltage is lesser than the inverting input voltage. So, the output goes to -ve saturation level($-V_{sat}$)
- Saturation ⟶ equal to +ve (or) –ve supply voltage.

ZERO CROSSING DETECTORS:

It is defined as the output will change from one state to another very rapidly every time when the input signal passes through zero.



The circuit diagram and input-output waveforms of zero cross detector are shown in above figure.

In the comparator if the inverting terminal is grounded then the comparator becomes zero crossing detector.

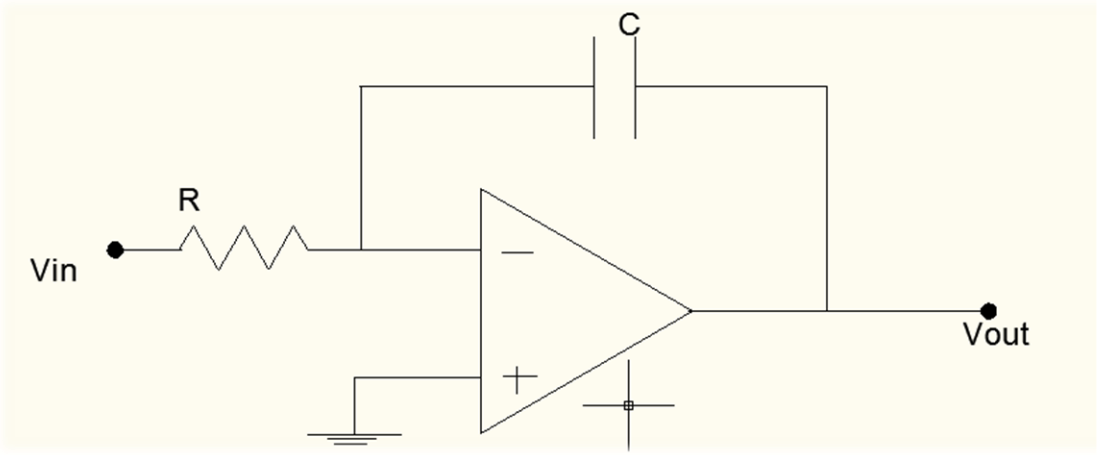
When compared with the period of the input signal the time constant of RC network is very small. The comparator output is a rectangular signal with respect to the input signal. Hence it is also ***called as the sine to square wave converter.***

The differentiator (R and C) output contains a series of positive and negative pulses. The diode D rectifies this signal and hence the output contains only the positive pulses.

Therefore, Positive pulses are produced at its output at the time of input signals cross from negative voltage to positive voltage through zero. If we reverse the diode direction, the output contains only negative pulses. These pulses are produced at its output at the time of input signals cross from positive side to negative side through zero.

INTEGRATOR:

An integrator circuit integrates the input signal with respect to time (frequency).



The circuit diagram of integrator is shown in the above figure. The feedback element is capacitor and the input element is resistor.

The charge on a capacitor C, when a supply voltage of V applied is Q = CV. In general, the current through the capacitor,

$$I_c = \frac{dQ}{dt} = \frac{dCV}{dt} = \frac{CdV}{dt}, \text{since C is constant}$$

By using Kirchhoff's current law in the circuit.

$$i_1 = i_f$$

The current flows through the resistor R $\longrightarrow i_1$

The current flows through the capacitor C $\longrightarrow i_f$

$$\frac{V_i - V_s}{R} = C\,\frac{dV}{dt}$$

$$\frac{V_i - V_s}{R} = C\,\frac{d(V_s - V_0)}{dt}$$

Since V_s=0 (it is virtual ground)

$$\frac{V_i}{R} = -C\,\frac{dV_0}{dt}$$

$$\frac{\mathrm{dV_0}}{\mathrm{dt}} = -\frac{\mathrm{V_i}}{\mathrm{RC}}$$

Integrating on both sides with respect to time

$$\mathrm{V_0} = -\frac{1}{\mathrm{RC}}\int \mathrm{V_i} + \mathrm{Vk(0)}$$

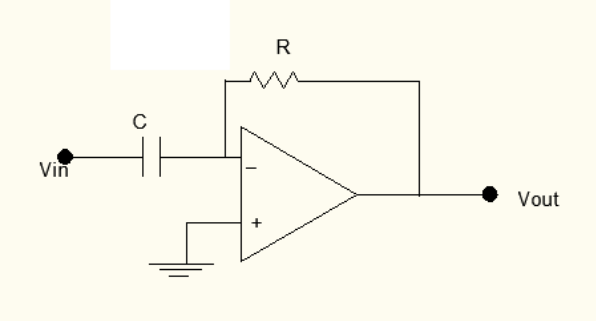
Where Vk(0) is the initial voltage produced at the output.

- For a square wave input, it produces triangular output waveform.
- For a sine wave input, it produces cosine output waveform.

The integrator is most commonly used in analog computers and A/D converters.

DIFFERENTATOR:

It produces the output signal, which is the derivative of input signal V_i.



If the resistor and capacitor of an integrator are interchanged, it will act as differentiator. The circuit diagram of differentiator is shown in above figure.

The charge on a capacitor C, when a supply voltage of V applied is Q=CV.

The current flow through the capacitor $I_c \longrightarrow$

The feedback current $\longrightarrow I_f$

By using Kirchhoff's current law

$$i_c = i_f$$

$$\frac{C\ d(V_i - V_s)}{dt} = \frac{V_s - V_0}{dt}$$

V_s = 0, because it is a virtual ground;

$$\frac{CdV_i}{dt} = -\frac{V_0}{R}$$

$$\frac{V_0}{R} = -\frac{CdV_i}{dt}$$

$$V_0 = -RC\frac{dV_i}{dt}$$

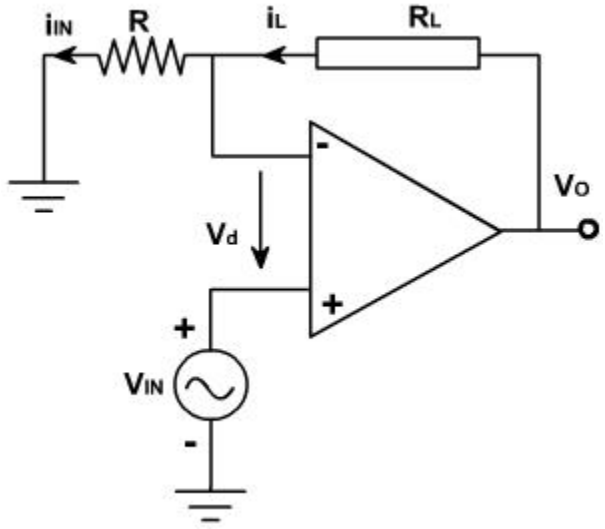
The output signal is the differentiation of input signal with respect to time.

- For a square wave input, it produces spike output.
- For a cosine wave input, it produces sine wave output.
- For a triangular wave input, it produces square wave output.

VOLTAGE TO CURRENT CONVERTER (Transconductance amplifier)

In voltage to current converter, ***the output current is proportional to input voltage.*** The voltage to current converter is also called as Transconductance amplifier**.** There are two types of circuits are possible in voltage to current converter. They are

i) V to I converter with floating load
ii) V to I converter with grounded load.



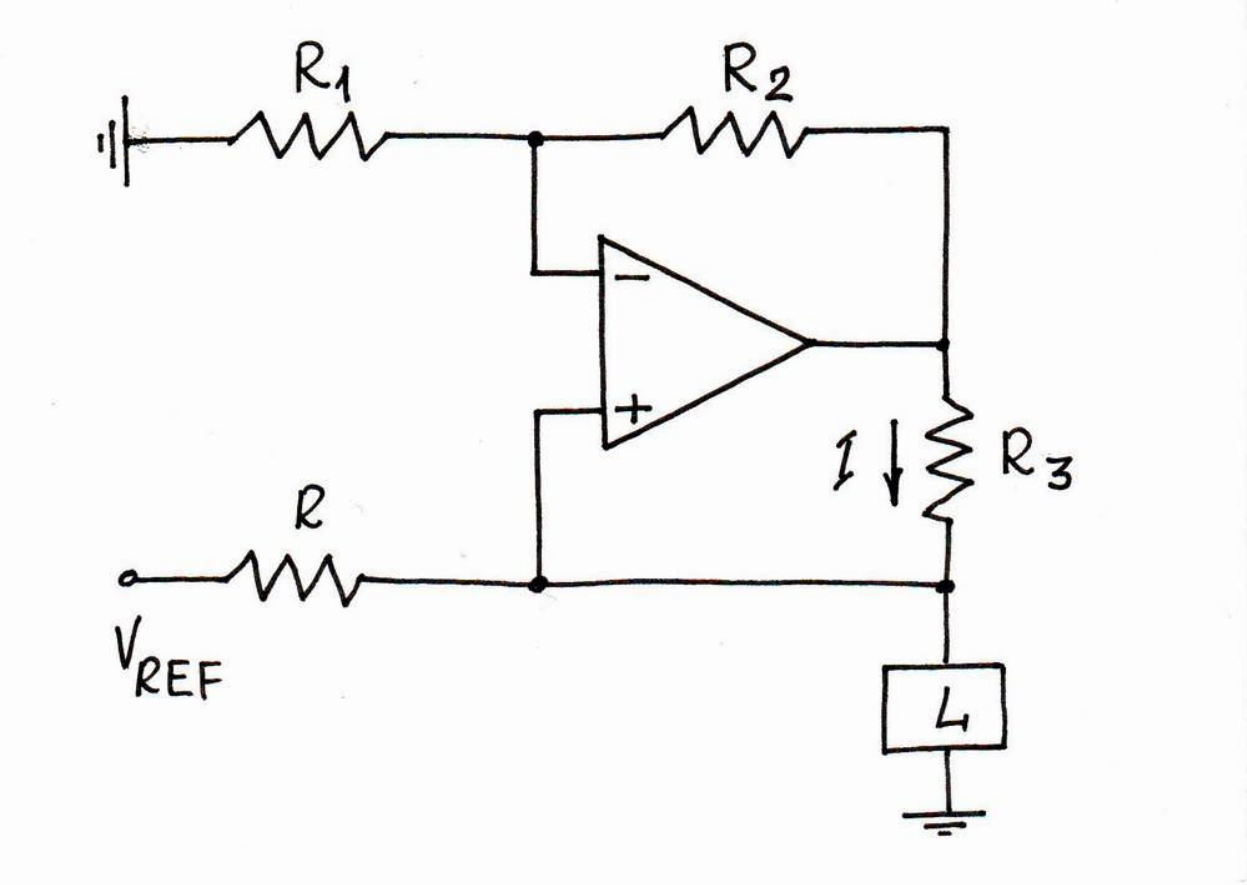
The circuit diagram of voltage to current converter with floating load is shown in above figure. The voltage at node 'a' is equal to V_i.

Therefore, $V_i = i_L R_i$

$$\therefore i_L = \frac{V_i}{R_i} = KV_i \left(\therefore \frac{1}{R_i} = K\right)$$

$$i_L \propto V_i$$

Hence, the output (load) current is directly proportional to the input voltage.



A voltage to current converter with grounded load is shown in above figure.

Writing KCL, we get, $i_1 + i_2 = i_L$

$$\frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = i_L$$

$$\frac{V_i - V_1 + V_0 - V_1}{R} = i_L$$

$$\frac{V_i - 2V_1 + V_0}{R} = i_L$$

$$V_i + V_0 - 2V_1 = i_L R$$

$$2V_1 = V_i + V_0 - i_L R$$

$$V_1 = \frac{V_i + V_0 - i_L R}{2}$$

Since the op-amp is used in non-inverting mode, the gain of the amplifier

$$A_v = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_i}$$

Assume, $R_f = R_i = R$

$$\frac{V_0}{V_i} = 1 + \frac{R}{R}$$

$$\frac{V_0}{V_i} = 1 + 1 = 2$$

$$V_0 = 2\,V_i$$

Assume $V_i = V_1$

The output voltage is $V_0 = 2V_1$

Now substitute the value of V_1

$$V_0 = 2\left(\frac{V_i + V_0 - i_L R}{2}\right)$$

$$V_0 = V_i + V_0 - i_L R$$

$$V_0 - V_0 = V_i - i_L R$$

$$0 = V_i - i_L R$$

$$V_i = i_L R$$

$$\text{so, } i_L = \frac{V_i}{R}$$

$$i_L = KV_i \left(\therefore K = \frac{1}{R}\right)$$

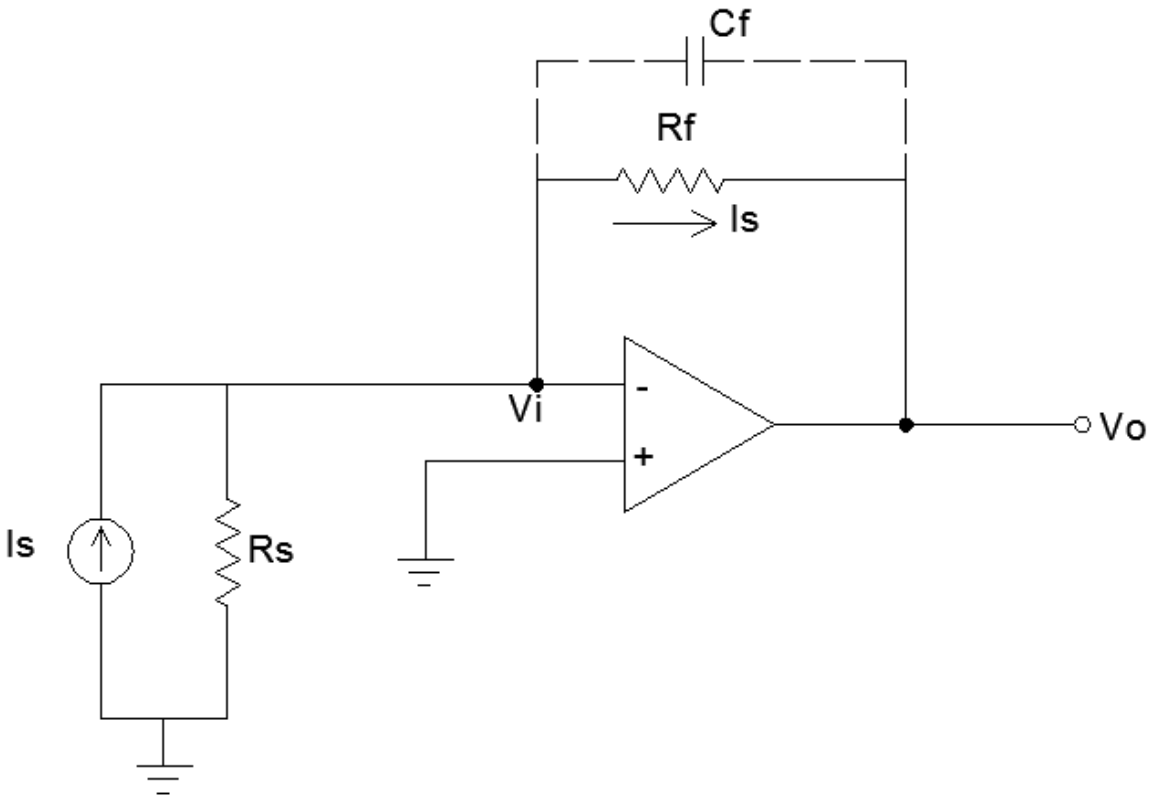
$$i_L \,\alpha\, V_i$$

Hence the output load current is directly proportional to the input voltage.

CURRENT TO VOLTAGE CONVERTER: (Transimpedance amplifier)

It produces ***output voltage is proportional to the input current***

The circuit diagram of current to voltage converter is shown in given figure. Since the (-) negative input terminal is at virtual ground, no current flows through R_s and current are flows through the feedback resistor R_f.



In this circuit $I_s = \frac{V_i - V_0}{R_f}$

$$V_i = 0$$

$$I_s = \frac{-V_0}{R_f}$$

$$V_0 = -I_s R_f$$

$$(\therefore K = -R_f)$$

$$V_0 = -I_s K$$

$$V_0 \alpha I_S$$

It is also called Transresistance amplifier. The capacitor (C_f) is used to reduce high frequency noise and the possibility of oscillations.

INSTRUMENTATION AMPLIFIER:

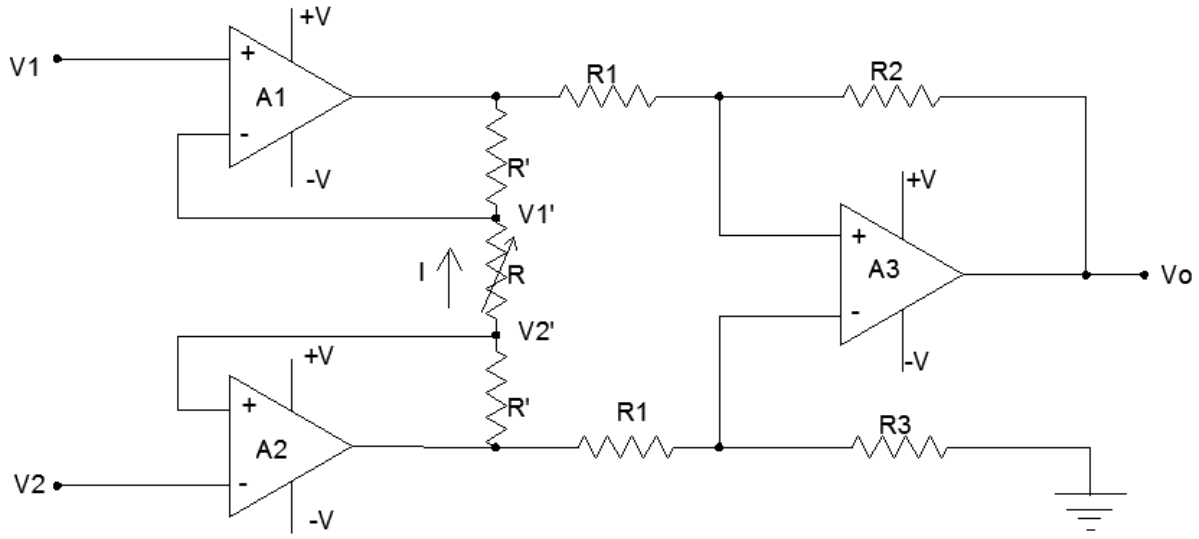
DEFINITION:

An instrumentation amplifier is a differential op-amp circuit providing high input impedances with ease of gain adjustment through the variation of a single resistor.

WORKING:

The transducers are required to measure and control physical quantities in the field of analog instrumentation. The transducers output has to be amplified in order to drive the indicator or display system. For this purpose, an instrumentation amplifier is used.

The circuit diagram of instrumentation amplifier is shown in given figure.



INSTRUMENTATION AMPLIFIER

WORKING:

- The op-amp A_1 and A_2 have zero differential input voltage.
- For $V_1=V_2$(common mode condition), the voltage across R will be zero. So, no current flow through R and R'. Then the non-inverting amplifier A_1 acts as voltage follower. Its output voltage, $V_1' = V_1$.
- Similarly op-amp A_2 acts as voltage follower having output $V_2' = v_2$.
- However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2' - V_1') > (V_2 - V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op amp.

The gain of op-amp A3 with respect to V2' and V1',

$$V_0 = \frac{R_2}{R_1}(V_2' - V_1') \dots\dots\dots (1)$$

Since no current flows into the op amp, the current flowing in resistor,

$$I = \frac{V_2 - V_1}{R}$$

It passes through the resistor R'

$$\therefore V_2' = IR' + V_2$$

Now, Substitute the value of I

$$V_2' = \frac{R'}{R}(V_2 - V_1) + V_2 \quad \ldots\ldots\ldots (2)$$

Similarly$V_1' = V_1 - IR'$

$$V_1' = V_1 - \frac{R'}{R}(V_2 - V_1) \quad \ldots\ldots\ldots (3)$$

Putting the values of V_1' and V_2' in equation (1)

We obtain,

$$V_0 = \frac{R_2}{R_1}\left(\frac{R'}{R}(V_2 - V_1) + (V_2 - V_1) + \frac{R'}{R}(V_2 - V_1)\right)$$

Let us commonly take $(V_2 - V_1)$ outside,

$$= \frac{R_2}{R_1}(V_2 - V_1)\left(\frac{R'}{R} + 1 + \frac{R'}{R}\right)$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_2 - V_1)$$

Requirements of a Good Instrumentation Amplifier

- Finite, Accurate and Stable Gain
- Easier Gain Adjustment
- High Input Impedance:
- Low Output Impedance
- High CMRR
- High Slew Rate

Advantages of Three Op-amp Instrumentation Amplifier:

- The gain can be easily varied and controlled by adjusting the value of Rgain without changing the circuit structure.

- The gain depends upon the external resistors used. Hence, the gain can be accurately set by choosing the resistor values carefully.
- The input impedance is dependent on the non-inverting amplifier circuits at the input stage. It is very high.
- The output impedance is nothing but the output impedance of the difference amplifier, which is very low.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

FEATURES OF INSTRUMENTATION AMPLIFIER:

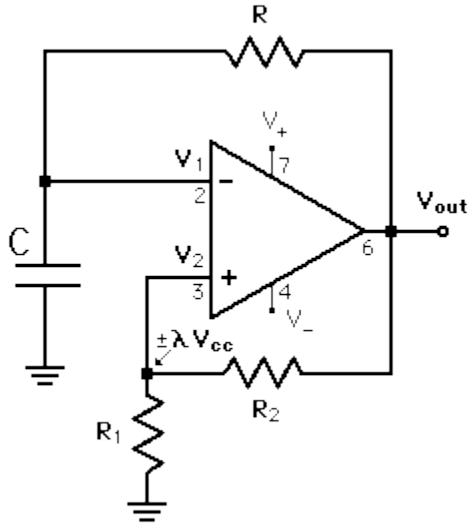
- ❖ High gain accuracy
- ❖ High CMRR
- ❖ High gain stability
- ❖ Low DC offset
- ❖ Low output impedance

WAVEFORM GENERATORS:

The various op-amp circuits used for generating various waveforms such as square, triangular, saw tooth, sine etc. are called signal generators or waveform generators. Waveform generators produce a time dependent signals with required frequency, amplitude and wave shape.

SQUARE WAVE GENERATOR:

A simple square wave generator by using op-amp is shown in given figure. It is otherwise called astable multivibrator or a free running oscillator.



A capacitor is connected at is inverting input terminal .It is basically a comparator circuit. So the output goes to either $+V_{sat}$ or $-V_{sat}$, depending upon its differential input voltage. By connecting the portion divider across the output terminal, a portion of output voltage (βV_{sat}) is applied to the non-inverting input of op-amp.

From the figure, now we are going to calculate the output voltage starting from ground.

$$\frac{0 - V_2}{R_2} = \frac{V_2 - V_0}{R_1}$$

$$\frac{-V_2}{R_2} = \frac{V_2 - V_0}{R_1}$$

$$\frac{-V_2}{R_2} = \frac{V_2}{R_1} - \frac{V_0}{R_1}$$

$$\frac{V_0}{R_1} = \frac{V_2}{R_1} + \frac{V_2}{R_2}$$

$$\frac{V_0}{R_1} = V_2\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

Now take LCM,

$$\frac{V_0}{R_1} = V_2\frac{R_1 + R_2}{R_1 R_2}$$

$$\frac{1}{R_1}\left(\frac{R_1 R_2}{R_1 + R_2}\right) = \frac{V_2}{V_0}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_2}{V_0}$$

$$V_2 = V_0\left(\frac{R_2}{R_1 + R_2}\right)$$

Assume,

$$\beta = \left(\frac{R_2}{R_1 + R_2}\right)$$

$$V_2 = \beta V_0$$

That is β amount of output voltage is fed back to non-inverting input terminal.

Due to the mismatch between the inverting and non-inverting terminals of the op-amp, the output goes to either $+V_{sat}$ or $-V_{sat}$.

- When the supply voltage is switched ON, assume that the output goes to $+V_{sat}$. Due to this, $+\beta V_{sat}$ is applied to the non-inverting input of op-amp.
- Then the capacitor C starts charging with a polarity of upper plate positive and lower plate negative towards $+V_{sat}$ through resistor R.

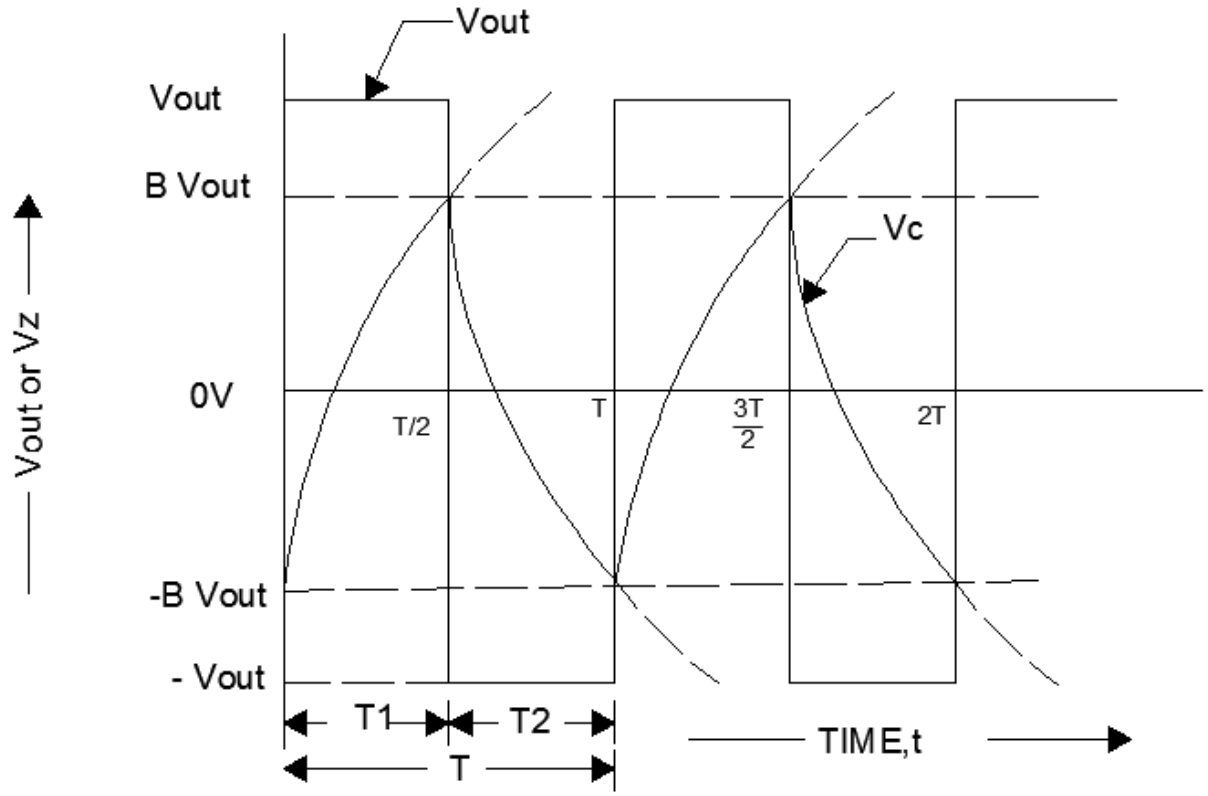
- When the capacitor reaches $+\beta V_{sat}$, the output goes to $-V_{sat}$.

- Now $-\beta V_{sat}$voltage is applied to the non-inverting input of op-amp.

- Then the capacitor starts charging in opposite direction, with lower plate positive and upper plates negative towards $-V_{sat}$through the resistor R.

- Similarly when the capacitor attains $-\beta V_{sat}$the output of op-amp goes to +Vsat , and $+\beta V_{sat}$ is applied to its non-inverting terminal. And the process repeated.

- The signal waveform of square wave generator is shown in figure.



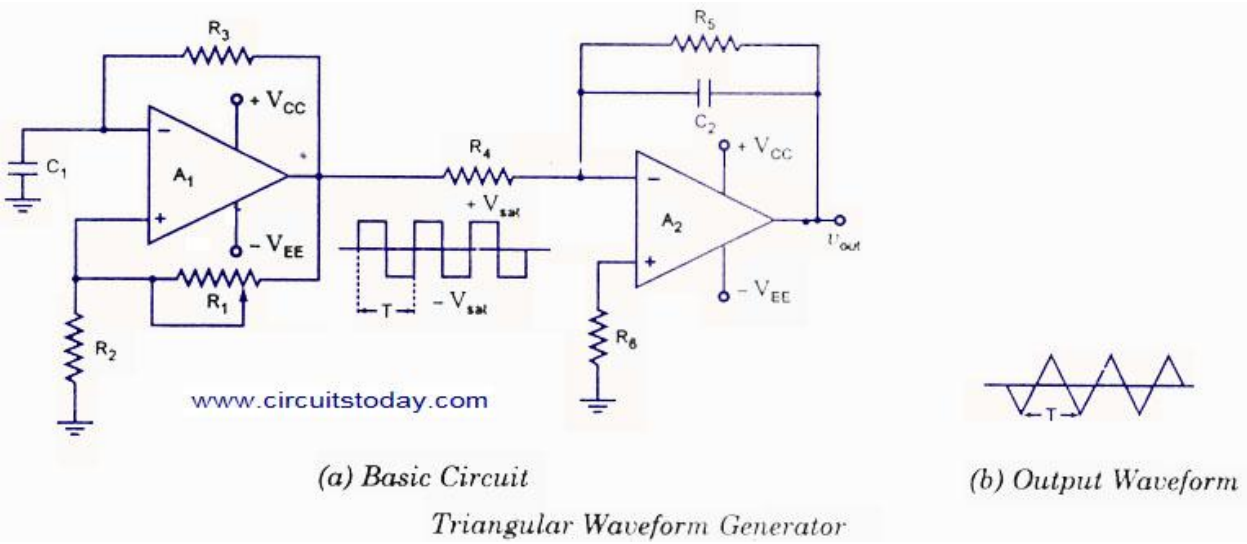
OUTPUT AND CAPACITOR VOLTAGE WAVEFORM

A continuous square wave signal is generated at the output with respect to the charging and discharging effect of capacitor.The total time period for one oscillation is given as

$$\mathbf{T = 2RC\ ln\left(\frac{2R_1 + R_2}{R_2}\right) sec}$$

TRIANGULAR WAVE GENERATOR:

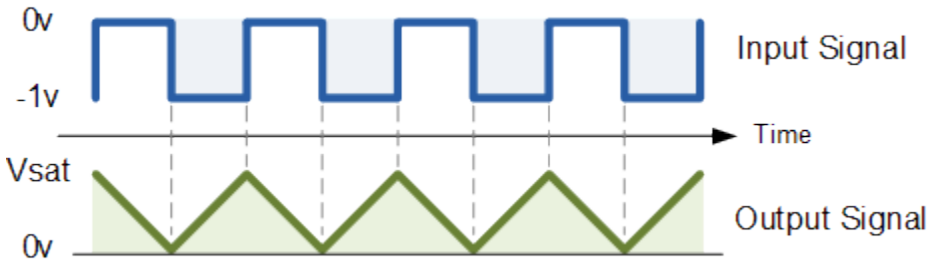
By connecting an integrator circuit at the output of square wave generator, triangular wave will be generated.



(a) Basic Circuit *(b) Output Waveform*

Triangular Waveform Generator

The amplitude of square wave generator is constant at $\pm V_{sat}$. But in triangular wave, amplitude will decrease as the frequency increases. This is due to the reactance of capacitor C_2 in the feedback circuit. Aresistance R_4 is connected across C_2 to avoid saturation problem at low frequencies. But the frequency of the triangular wave is same as that of square wave.



The square wave at the output of square wave generator is converted into triangular wave signal with respect to the charging and discharging effect of capacitor.

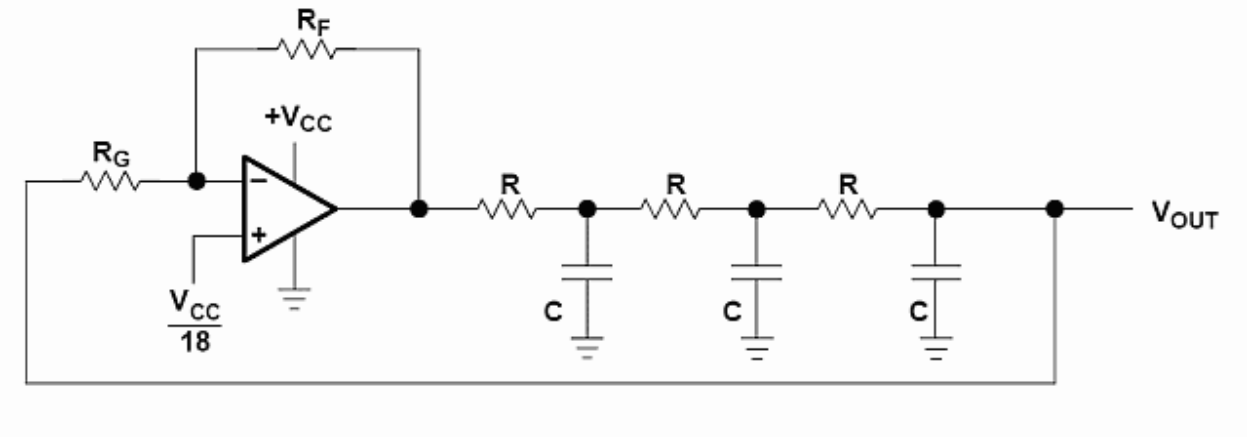
- When V' is low at $-V_{sat}$, it forces a constant current $\left(-\frac{V_{sat}}{R_3}\right)$through C_2 (right to left) to drive V_o positive linearly.
- Because, the output of square wave generator is applied to the inverting input of integrator.
- Similarly, when V' is high at $+V_{sat}$, forces constant current $\left(+\frac{V_{sat}}{R_3}\right)$through C_2 (left to right) to drive V_o negative linearly.

The frequency of oscillation can be given as,

$$\mathbf{f_0 = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}}$$

SINE WAVE GENERATOR:

The circuit diagram of RC phase shift oscillator using op-amp for producing sinusoidal signal is shown in given figure.



- RC phase shift oscillator using op-amp uses op-amp in inverting amplifier mode.
- Thus it introduces the phase shift of 180° between the input and output.
- The feedback network produces another 180°. So the total phase shift is 360°.
- In the feedback loop three RC networks are used. So each RC network produces 60°phase shift.
- This satisfies the required conditions for positive feedback and circuit works as an oscillator.

  The frequency of the signal produced by this oscillator, $\mathbf{f = \frac{1}{2\pi RC\sqrt{6}}}$

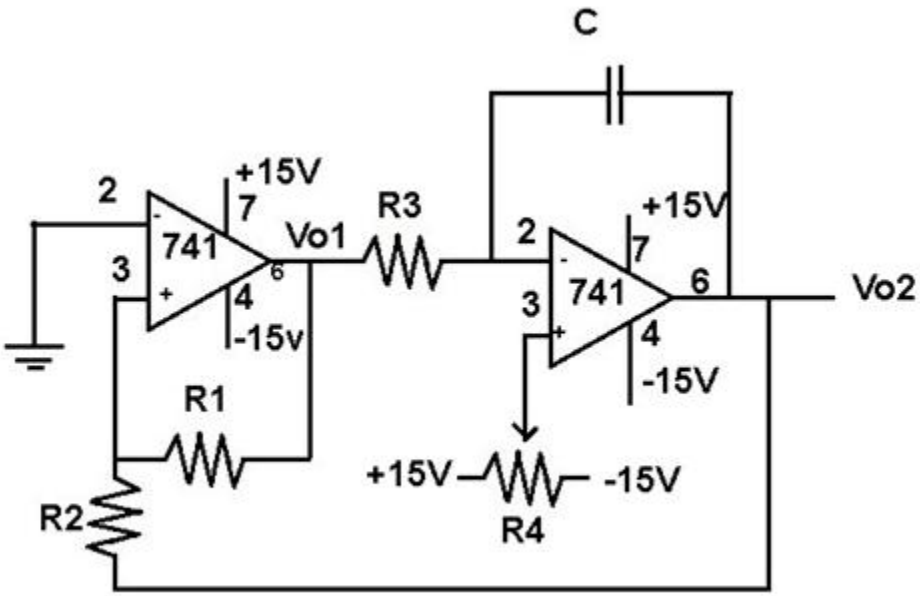
Advantages:

- ❖ The circuit is easy to design.
- ❖ It produces output over audio frequency range.
- ❖ It is a fixed frequency oscillator.

Disadvantage:

It cannot be used for tuned oscillator.

SAW TOOTH GENERATOR:



Triangular wave has equal rise and fall times but a saw tooth wave rises positively than it falls or it falls many times faster than it rises.Therefore, a triangular wave generator can be converted into a saw tooth wave generator by connecting a variable dc voltage into the non-inverting terminal of integrator, as shown in above figure.

Here, the non-inverting terminal (+input) of the integrator is driven by the voltage set between $+V_{CC}$ to $-V_{EE}$ by the potentiometer R4. Depending on the R4 setting, a certain dc level is added in the output of integrator.

As output of the integrator decides the effective voltage at point P, added dc level in the output of the integrator will affect the duty cycle of the comparator output. When the voltage at the non-inverting input of the integrator is negative, the duty cycle is less than 50%, resulting longer rise time than the fall time.

On the other hand, when voltage at the non-inverting input of the integrator is positive, the duty cycle is greater than 50% and rise time is less than the fall time.

The frequency of the saw tooth generator decreases, when the voltage at the non-inverting input of the integrator B is adjusted towards $+V_{CC}$ or $-V_{EE}$.

The amplitude of saw tooth wave is independent of the voltage setting at the non-inverting input of the integrator.

UNIT III

PLL and its applications

Introduction

Phase locked loop is an important building block in linear circuits. It was introduced in 1930 as a discrete circuit. In present, the PLL is now readily available as IC's which were developed in the SE/NE 560 series. Some of the commonly used ones are the SE/NE 560, 561, 562, 564, 565 and 567.The difference between each one of them is in the different parameters like operating frequency range, power supply requirements, and frequency and bandwidth ranges. Out of all the series, the SE/NE 565 is the most famous. It is available as a 14-pin DIP and also as a 10-pin metal can package.

Definition:

A **phase-locked loop** (**PLL**) is a control system that generates an output signal whose **phase** is related to the **phase** of an input signal.

Types of PLL

There are five types of PLL

1. Analog Phase-Locked Loop (APLL) also referred to as a linear phase-locked loop (LPLL)
2. Digital phase-locked loop (DPLL)
3. All Digital phase-locked loop (ADPLL)
4. Software phase-locked loop (SPLL[)]
5. Neuronal PLL (NPLL)

1. **Analog or linear PLL (APLL)**
   Phase detector is an analog multiplier. Loop filter is active or passive. Uses a Voltage-controlled oscillator (VCO).

2. **Digital PLL (DPLL)**
   An analog PLL with a digital phase detector (such as XOR, edge-trigger JK, phase frequency detector). May have digital divider in the loop.
3. **All digital PLL (ADPLL)**
   Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator (NCO).
4. **Software PLL (SPLL)**
   Functional blocks are implemented by software rather than specialized hardware.
5. **Neuronal PLL (NPLL)**
   Phase detector, filter and oscillator are neurons or small neuronal pools. Uses a rate controlled oscillator (RCO). Used for tracking and decoding low frequency modulations (< 1 kHz), such as those occurring during mammalian-like active sensing.

PLL Applications

- Demodulation of both FM and AM signals
- Stereo Decoders.
- Frequency synthesis that provides multiple of a reference signal frequency.
- Used in motor speed controls, tracking filters.
- Used in frequency shift keying (FSK) decodes for demodulation carrier frequencies.
- Recovery of small signals that otherwise would be lost in noise
- Recovery of clock timing information from a data stream such as from a disk drive
- Clock multipliers in microprocessors
- DTMF decoders, modems, and other tone decoders, for remote control and telecommunications
- DSP of video signals
- Atomic force microscopy

Basic Principle of PLL

The PLL consists of the following four main blocks.

1. Phase Detector / Phase Comparator
2. Low Pass Filter
3. Error Amplifier
4. Voltage Controlled Oscillator.

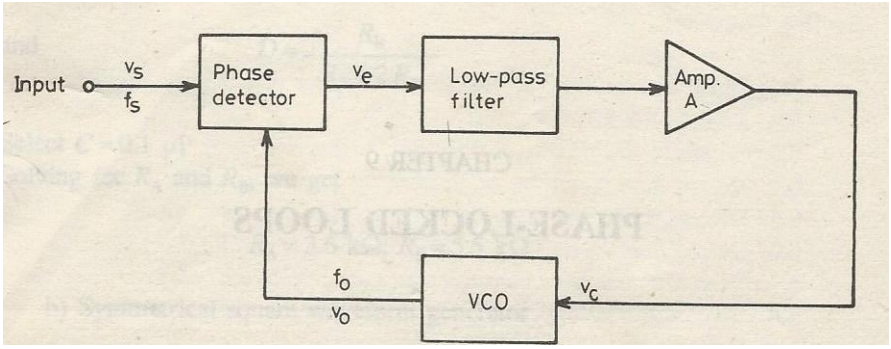


Fig (1)

In the forward loop, Phase comparator, Low pass filter and Error Amplifier are placed. In the feedback path, the VCO is placed.

The input signal Vs, with frequency fs, is applied to the PLL. The phase comparator compares the phase and frequency of this input signal, with the signal Vo from VCO with frequency fo.

Depending on the difference between the two signals, the phase comparator produces an error voltage Ve. It produces two frequencies (fo + fs) and (fo - fs). The higher frequency component is filtered by the LPF. The error voltage, called control voltage is fed to the VCO. This Ve shifts the VCO frequency so as to reduce the frequency difference between fs and fo.

Now the loop is said to be in the Capture range. The VCO keeps on changing its frequency till its frequency equals the input frequency i.e. fs = fo. Now the loop is said to be locked.

The output frequency fo, is equal to the input signal fs, with a finite phase difference ø.

If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

So, the PLL goes through the following three stages.

a. Free running
b. Capture and
c. Locked (or) tracking.

The capture transient is shown here

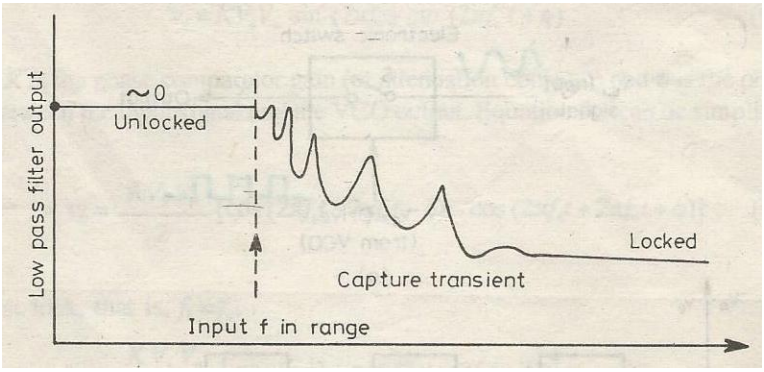


Fig (2)

When the PLL is in the unlocked condition, the Low pass filter delivers a constant output. As the capture range starts, due to the frequency difference between the input signal and the VCO frequency, a small sine wave appears at the output of LPF.

As the VCO frequency moves closer to the input frequency, the difference becomes smaller and it continues till the PLL locks.
After the lock has been obtained, the LPF, the VCO tracks the input signal very well.

When the VCO frequency is far away from the input signal, the beat frequency (fs ± fo) will be too high. So the LPF does not pass through this. So the signal is said to be in the "out of capture" range. Once locked the LPF has no control over the PLL. The VCO easily tracks the signal even just beyond the capture band.

Lock range:

The range of frequencies over which the Phase locked loop can maintain lock with the incoming signal is called lock – in range or tracking range. It is expressed as a percentage of fo, the VCO frequency.

Capture Range:

The range of frequencies over which the Phase Locker Loop acquire lock with the input signal is called capture range. It is expressed as a percentage of fo, the V.C.O frequency. The tracking range is always larger than the capture range.

Pull in time:

The total time taken by the loop to obtain lock is called pull in time. It depends on the initial phase and frequency difference between the two input signals, the overall loop gain and the loop filter characteristics.

Relation between the lock in range and capture range

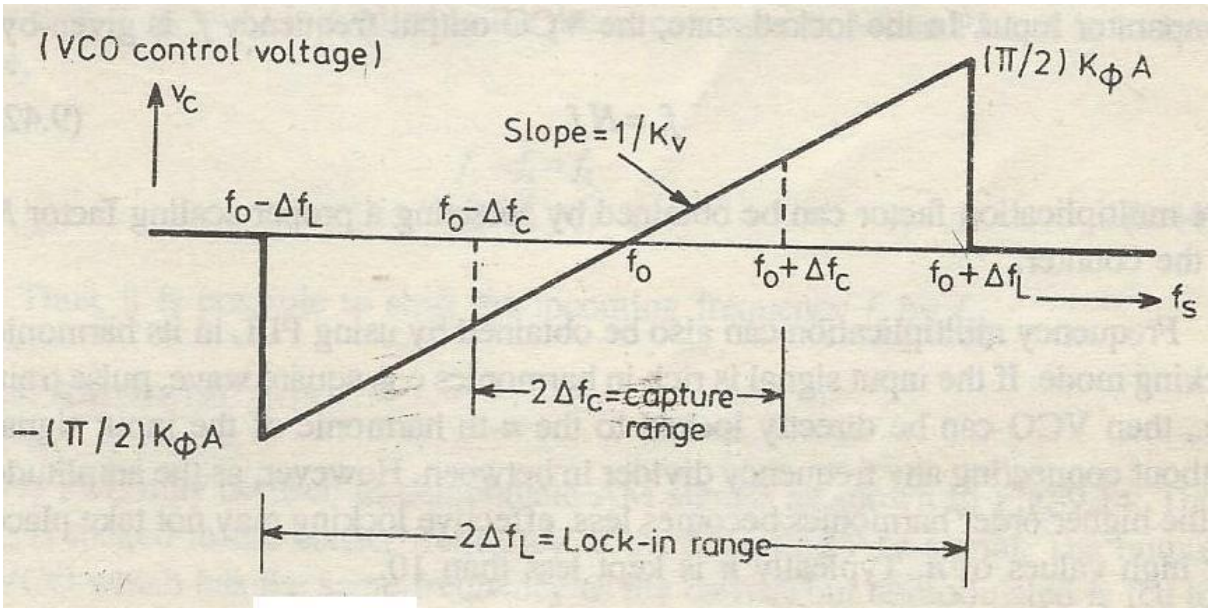


Fig (3)

Phase Detector / Phase Comparator

The comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies.

In other words, a phase detector or phase comparator is basically a frequency mixer (or) analog multiplier (or) logic circuit that generates a

voltage signal which represents the difference in phase between two signal inputs.

Types of Phase Detector

1. Analog type
   a. Electronic switch
   b. Doubled balanced mixer circuit (Balanced Modulator)
1. Digital type
   a. Using XOR
   b. Using S-R flip flop

1. Electronic Switch type Phase Detector

This is basically an electronic switch.. The switch is opened or closed by a square signal from VCO. Thus the input analog signal is chopped by the frequency determined by the VCO frequency. The switch is closed when the VCO output is positive and opens when the VCO output is negative.

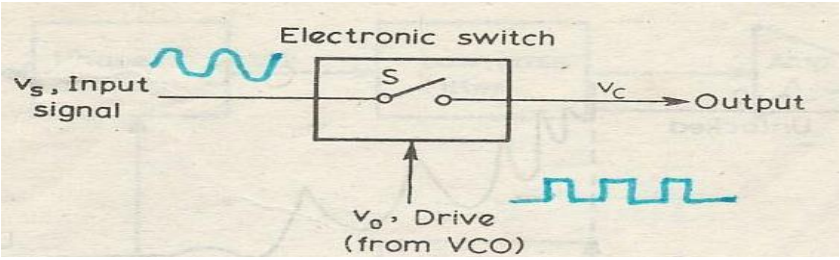
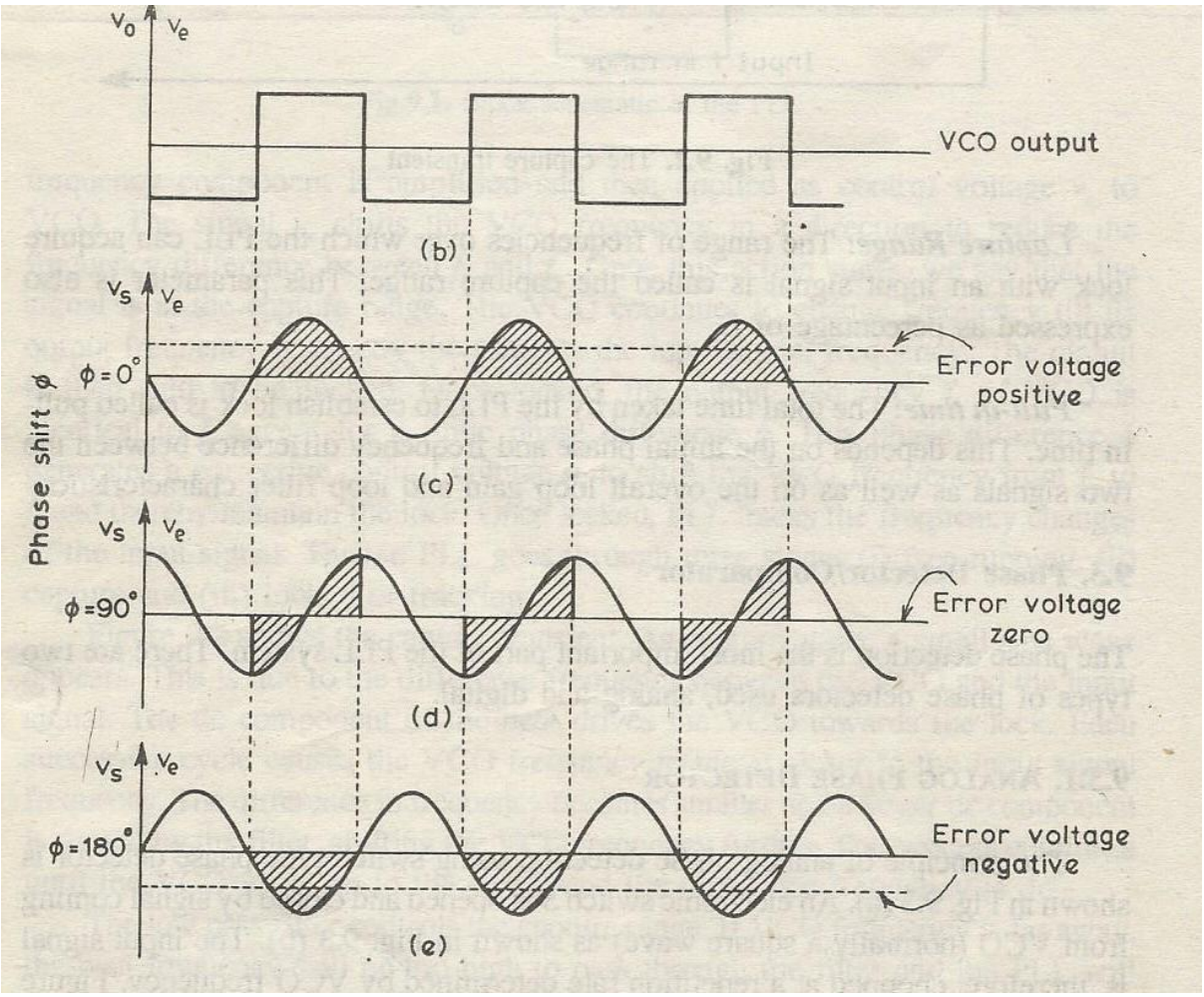


Fig (4)

1. When Vs and Vo are in phase (ø = 0): As the switch S is closed only for the positive output of VCO, the error voltage Ve is only the half positive portions of the input is permitted to cross the switch. Thus the average output i.e error voltage Ve is positive.
2. When Vs and Vo are out of phase by 90 (ø = 90): The switch closed for half of the Negative and the other half of the positive input. Thus the average output is zero. The error voltage Ve is zero.

3. When Vs and Vo are out of phase by 180 (ø = 180): The switch closed for negative half cycles of the input and opens for the positive half cycle of the input. Thus the average output is negative. The error voltage Ve is negative.

   The relation between the phase shift and Error voltage is shown here



Fig(5)

From the fig it is clear that

1. the error voltage is zero, when the phase shift between the two input is 90˚

2. the error voltage is positive, when the phase shift between the two input is < 90˚
3. the error voltage is negative, when the phase shift between the two input is > 90˚

In this type of Phase comparator, the phase information for only one half of the input waveform is detected and averaged. So, it is called as half wave detector. The output of the phase comparator is filtered and the error signal is obtained.

Draw backs of Switch type Analog Phase detector:

1. The output error voltage is proportional rp the input voltage. As it makes the phase detector gain and loop gain dependent on the input signal.
2. The output is proportional to cos ø and not proportional to ø, making it non linear.
   These two problems were removed by converting the input signal to a constant amplitude square wave.

Balanced Modulator type Analog Phase detector:

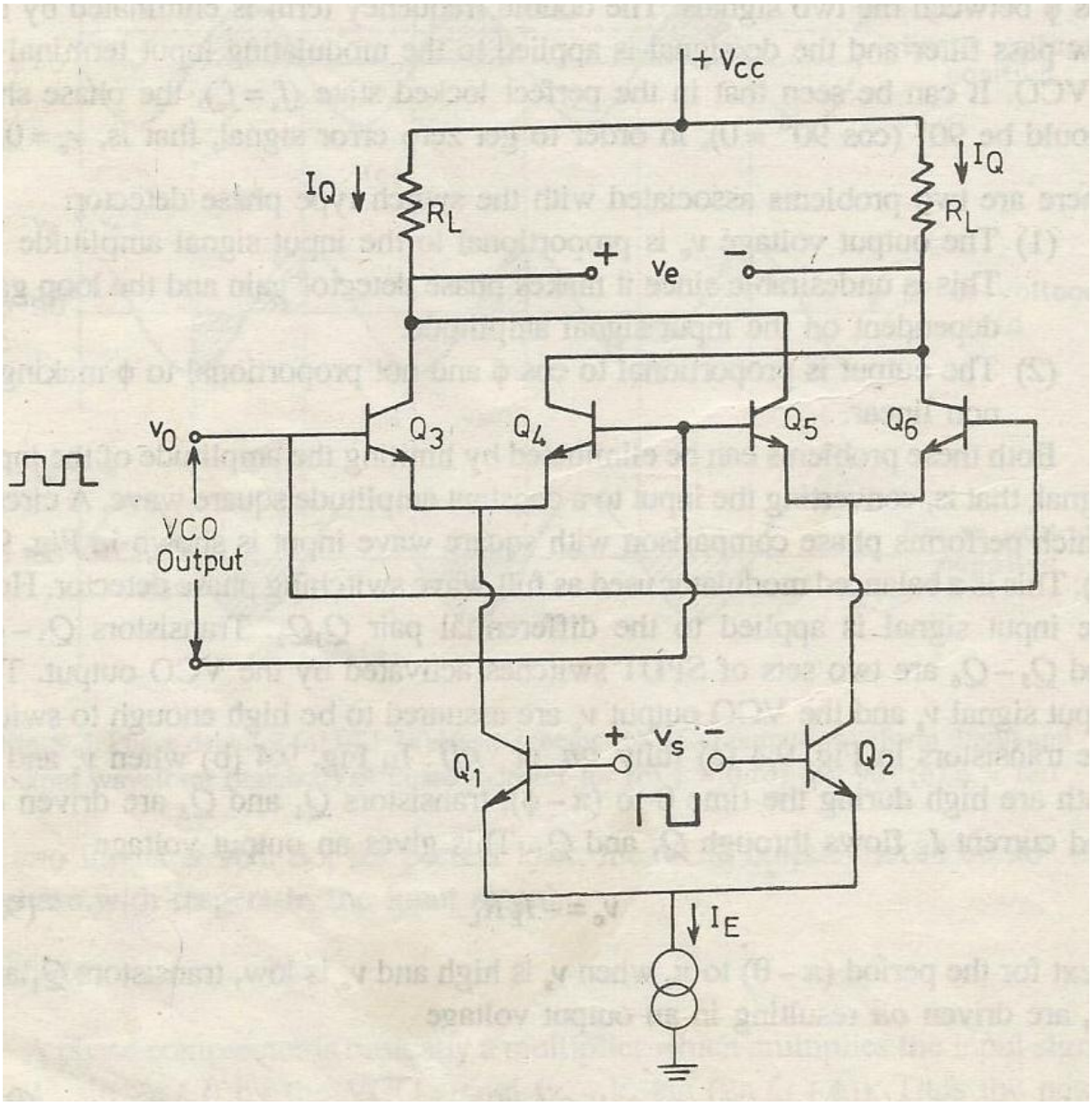


Fig (6)

In this type of comparator, the input is first converted into a constant amplitude square wave. As the phase information for the full wave is detected and averaged, it is called 'full wave detector'

It consists of a differential pair of transistors Q1-Q2 and two pairs (Q3- Q4) and (Q5-Q6) as SPDT switches.

The input to the differential pair is the input signal Vs. The SPDT switches are activated by the VCO output Vo. When these two inputs

are highly positive, the corresponding transistors are ON.. otherwise they are OFF.

When these two signals are high during the time 0 to (Π – ø) Q1 and Q3 are switched ON and a current Ie flows through Q1 and Q3. Therefore the output is given by Ve = - Ie X Re.

For the period (Π – ø) to Π, when Vs is high and Vo is low, Q1 and Q4 are driven to saturation and the output is Ve = Ie X Re.

Therefore as the phase difference moves from 0 to Π the output swings between +IeRe and –IeRe.

The linear relationship between Ve and ø is shown in fig.

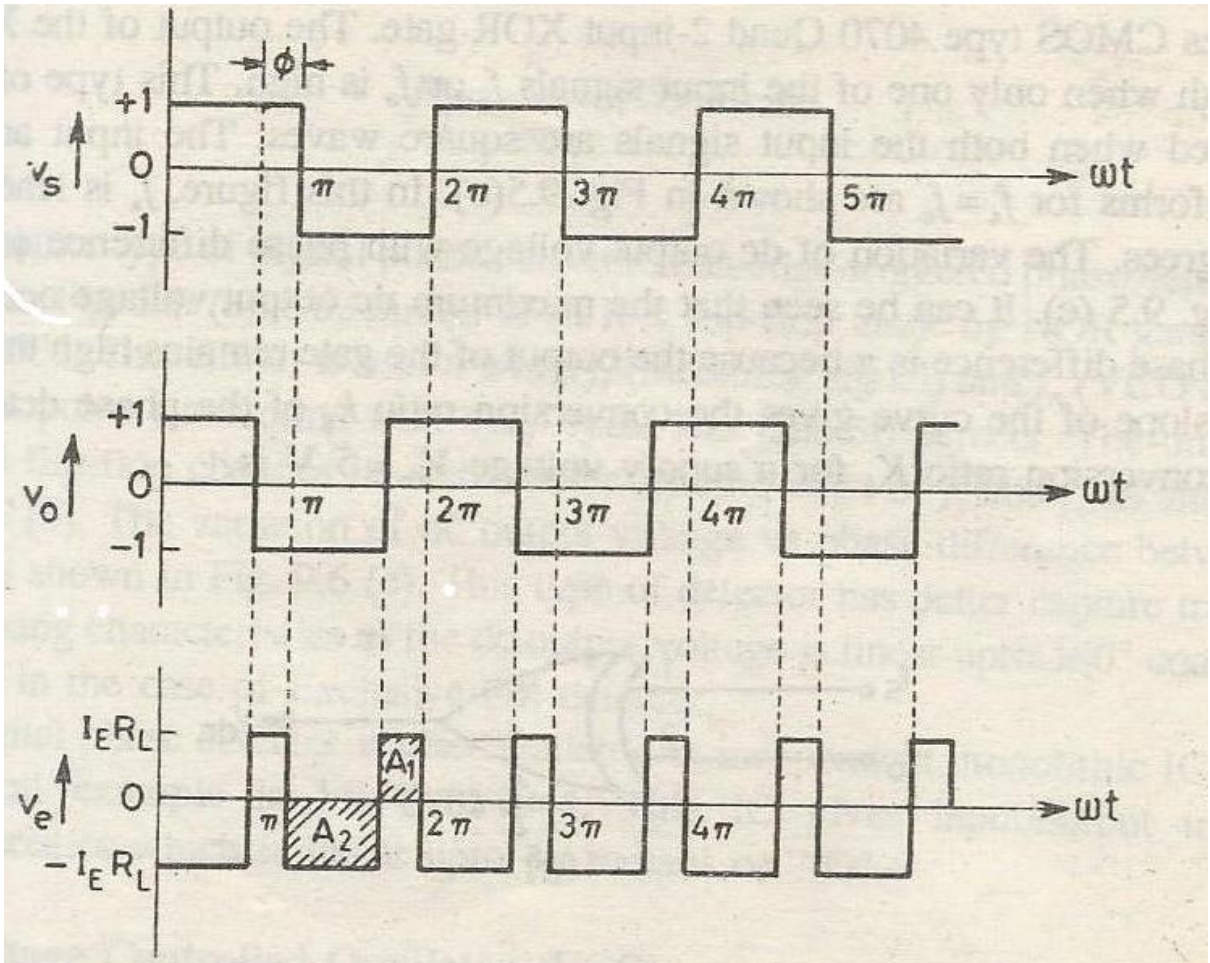


fig (7)

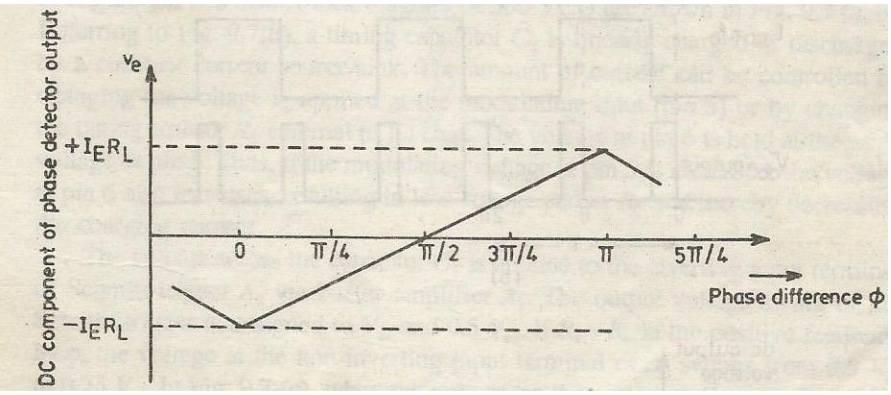
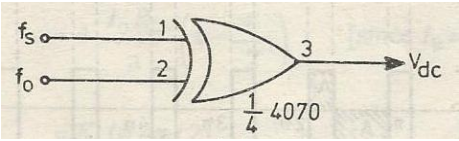


fig (8)

Digital Phase Detector

Exclusive OR Phase Detector

An exclusive OR phase detector is shown in the figure below.



Fig(9)

It is obtained as a CMOS IC of type 4070. Both the frequencies fs and fo are provided as an input to the EX OR phase detector. In EX-OR concept the output becomes HIGH only if either of the inputs fs or fo becomes HIGH. All other conditions will produce a LOW output.

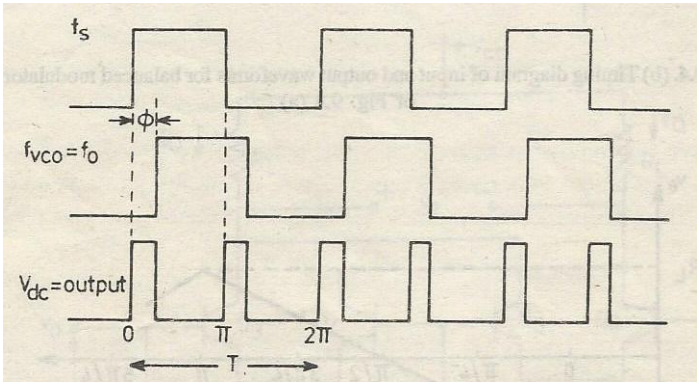
This type of detector is used when both the input signals fs and fo are square waves.

Let us consider a waveform where the input frequency leads the output frequency by ø degrees. (i.e) fs and fo has a phase difference of ø

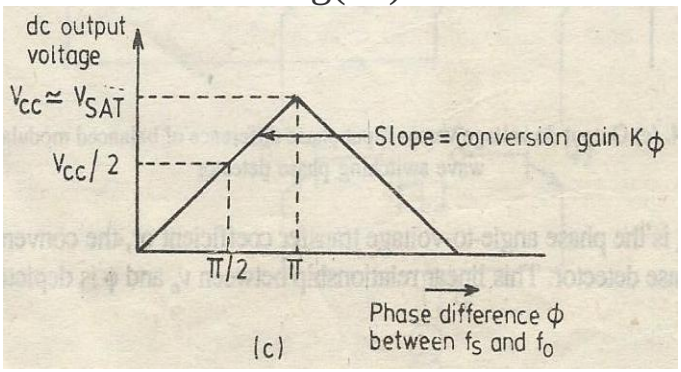
degrees. The dc output voltage of the comparator will be a function of the phase difference between its two inputs.

The figure shows the graph DC output voltage as a function of the phase difference between fs and fo. The output DC voltage is maximum when the phase detector is 180°.This type of phase detector is used when both fs and fo are square waves.

XOR phase detector waveforms



Fig(10)



Fig(11)

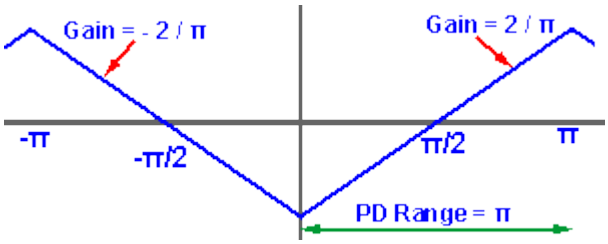
It can be seen that using these waveforms, the XOR gate can be used as a simple but effective phase detector.

Drawbacks of XOR phase detector:

The phase detector is sensitive to the clock duty cycle. This means that a steady duty cycle, i.e. 1:1 should be used. It will lock with a phase error, if the input duty cycles are not 50%.

- The output characteristic of the XOR PD show repetitions and gain changes. So, there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain.
- The nominal lock point with an XOR phase detector is also at the 90° static phase shift point.

The characteristic of the phase detector is as shown below:



XOR phase detector response curve

Unlike an analog mixer phase detector, the XOR version is

independent of input amplitude and constant over a Π phase range.

Digital Phase detector using Flip Flop

An edge triggered flip flop will very well act as a phase detector. This type of detectors are used when both the input wave and VCO output are pulses. And also if the duty cycle is less than 50%

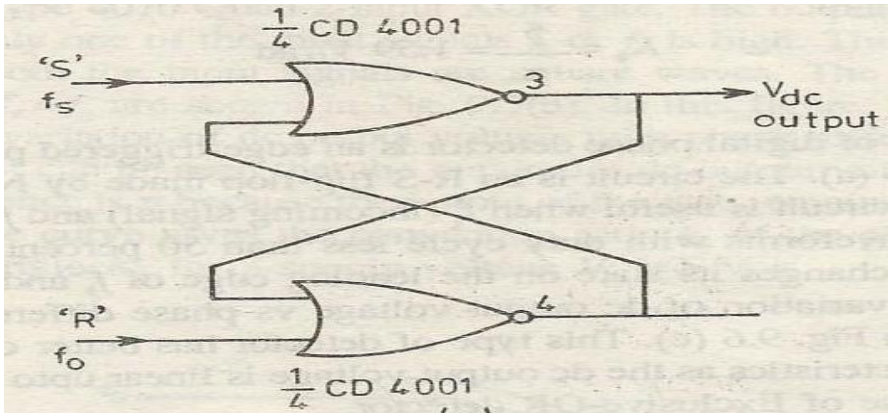
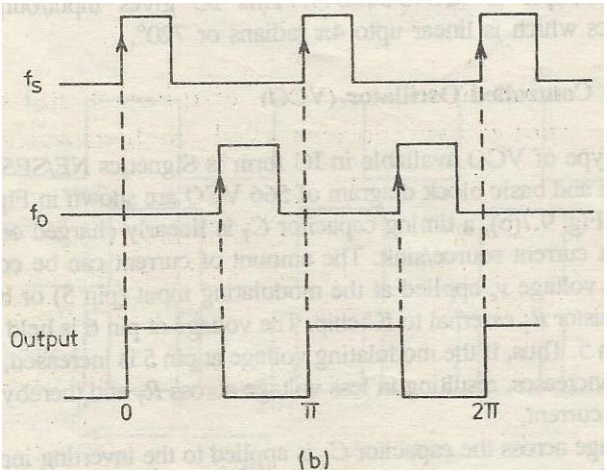


Fig (12)

A phase detector using NOR gates is shown here. It is a positive edge triggered flip-flop ie the change in output occurs when the clock input has a positive edge (low to high)

The input wave fs is fed to the S input. So the output becomes HIGH for the rising edge of the input signal.

The VCO output is fed to the R input of the flip flop. So the output becomes LOW for the rising edge of the VCO output.

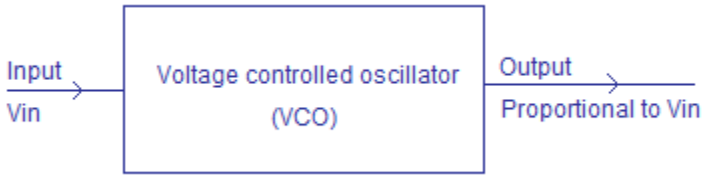


Fig(13)

As the duty cycle is less than 50% , a phase of 0˚ to 360˚ can be obtained. Therfore this type of detector has better capture tracking and locking characters than the XOR phase detectors.

VCO (Voltage controlled oscillator).

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. The Block diagram of a typical voltage controlled oscillator is shown below.



Voltage controlled oscillators can be broadly classified into

1. Linear voltage controlled oscillators and
2. Relaxation type voltage controlled oscillators.

Linear voltage controlled oscillators

Linear voltage controlled oscillators are generally used to produce a sine wave. In this type of oscillators, an LC tank circuit is used for producing oscillations. An active element like transistor is used for amplifying the output of the LC tank circuit. This active element compensates the energy lost in the tank circuit and establishes the necessary feedback conditions. Here, a varactor (varicap) diode is used in place of the capacitor in the tank circuit. Varactor diode is type of semiconductor diode whose capacitance across the junction

can be varied by varying the voltage across the junction. Thus by varying the voltage across the varicap diode in the tank circuit, the output frequency of the VCO can be varied.

Relaxation type voltage controlled oscillators

Relaxation type voltage controlled oscillators are used to produce a saw tooth or triangular waveform. This is achieved by the gradual charging and sudden discharge of a capacitor connected appropriately to an active element like UJT, PUT etc or a monolithic IC LM566 etc .Now a days, the relaxation type VCOs are generally realized using monolithic ICs.

VCO using OP –AMP

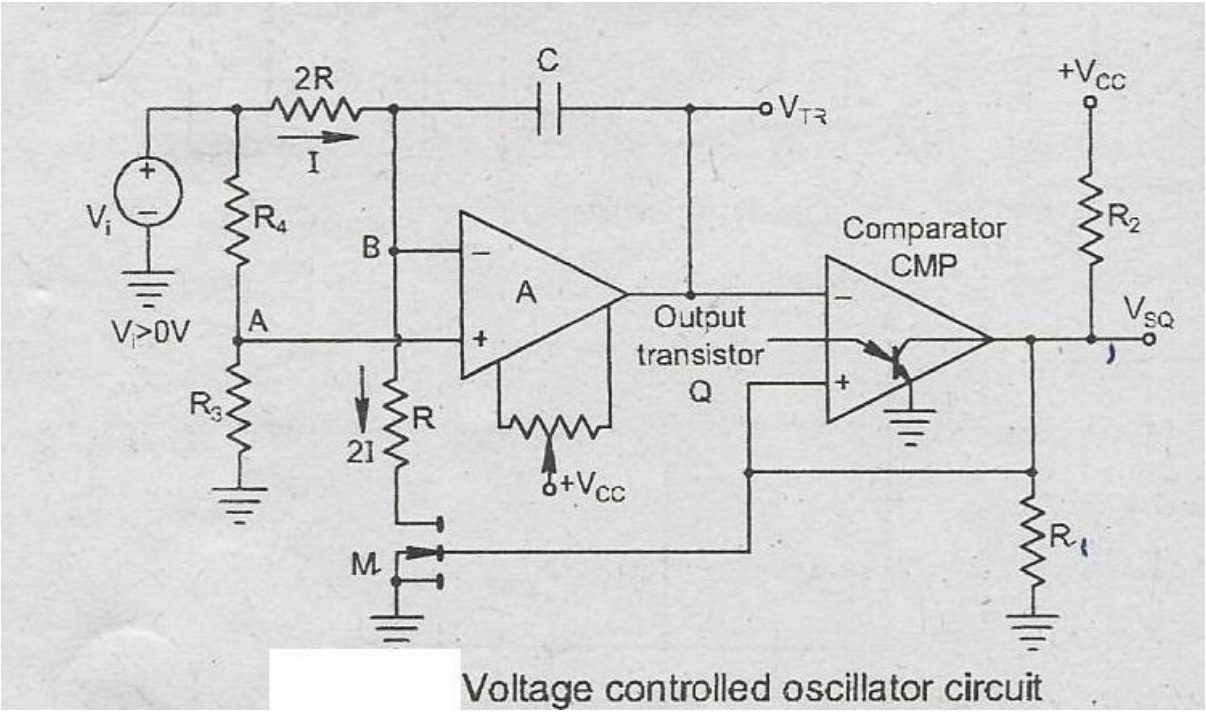


Fig (14)

This circuit uses two op –amps A1 and A2

Op-amp A1 is acting as a voltage to current converter, This circuit converts the input voltage into an output current. The output current is forced through the feedback capacitor. Therefore the output current is linear to the input voltage.

This output current is converted into triangular and square waveform using the second amplifier which is acting as a Comparator.

The direction of the current through the capacitor is controlled by the MOSFET switch. This switch is controlled by the comparator made up of Schmitt trigger.

When the comparator output is low, the switch M is off and the resistance becomes floating. Now th e capacitor charges from the input voltage.

When the comparator output is high, switch M is ON, and the resistance is grounded. So the capacitor discharges..

This circuit provides both triangular and square wave at a time..

When the output transistor Q is ON, the transistor is saturated, so the square output is low. The amplitude of the square wave is decided by the voltage divider R1 and R2.

When the square output is low, M is switched OFF. So the full current flows through the capacitor. Therefore the triangular voltage increases.

When the square output is high, the direction of the current changes and the triangular voltage decreases. This cycle repeats and a triangular wave form is generated.

Output waveform

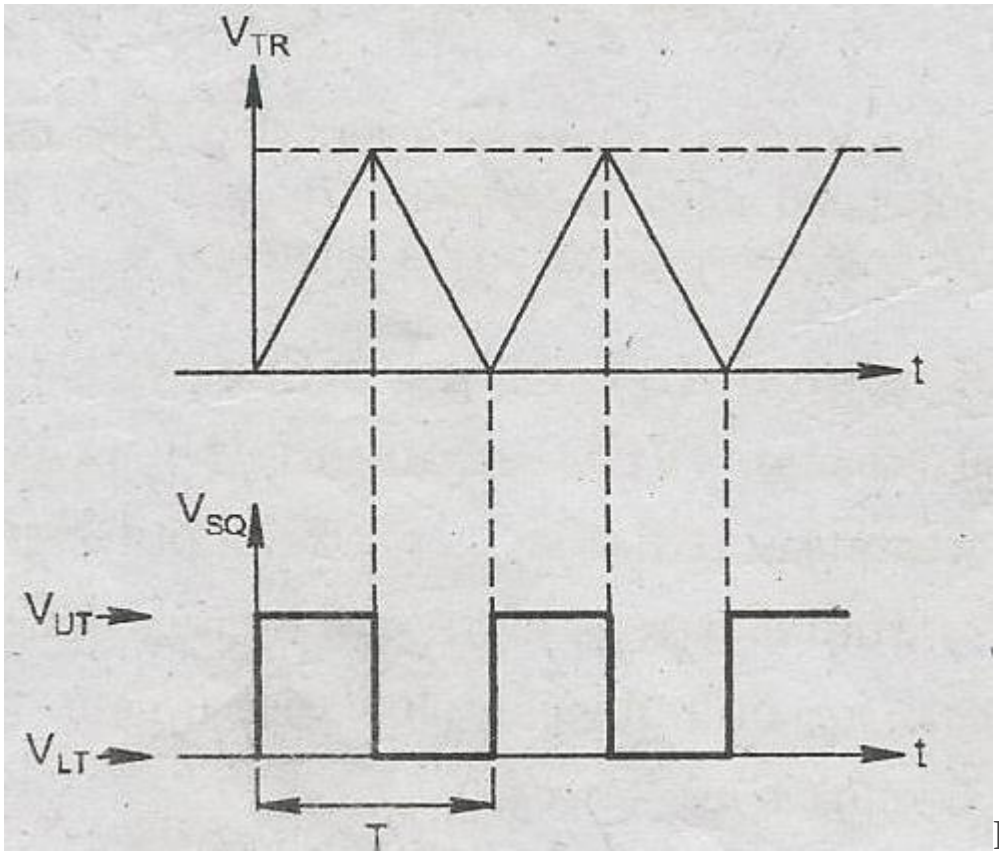


Fig (15)

2. Low Pass Filter (LPF)

A Low Pass Filter (LPF) is used in Phase Locked Loops (PLL) to get rid of the high frequency components in the output of the phase detector. It also removes the high frequency noise.

The primary function of the Low Pass Filter is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at start up.

The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input.

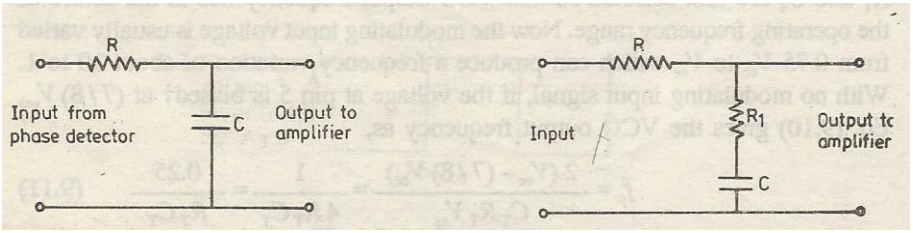
All these features make the LPF, a critical part in PLL and helps to control the dynamic characteristics of the whole circuit. The dynamic

characteristics include capture and lock ranges, bandwidth, and transient response.

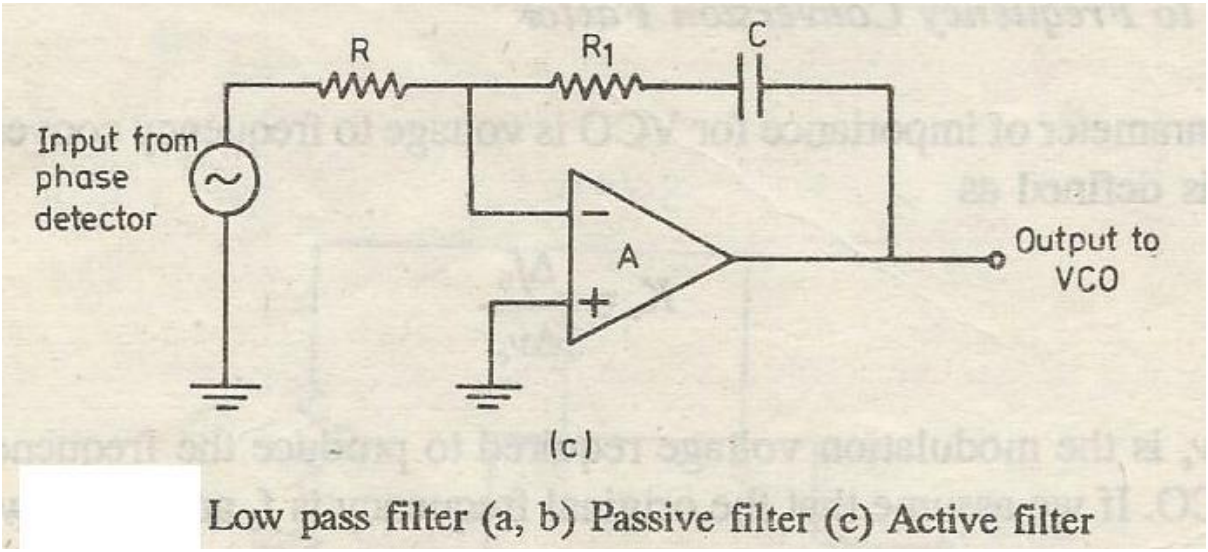
When the filter bandwidth is reduced, the response time increases .But this reduces the capture range. But it also helps in reducing noise and in maintaining the locked loop through momentary losses of signal. Thus it acts like a short time memory.

When the signal is lesser than the noise, the dc voltage in the capacitor will shift the VCO frequency continuously. This continues till the input signal comes back to its original amplitude. SO noise is reduced and locking stability is increased.

Two types of passive filter are used for the LPF circuit in a PLL. An amplifier is used also with LPF to obtain gain. The active filter used in PLL is shown below



Fig(17)



Low pass filter (a, b) Passive filter (c) Active filter

Pin details of VCO - IC 566

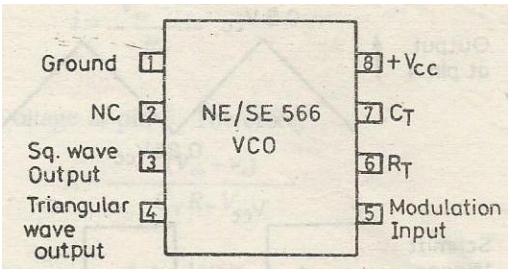


fig (16)

LM566 is a monolithic voltage controlled oscillator, from National semiconductors. It can be used to generate square and triangle waveforms simultaneously. The frequency of the output waveform can be adjusted using

(i) the external resistor Rt

(ii) the external capacitor Ct

(iii) the modulating voltage Vc

Basic block diagram of VCO 566

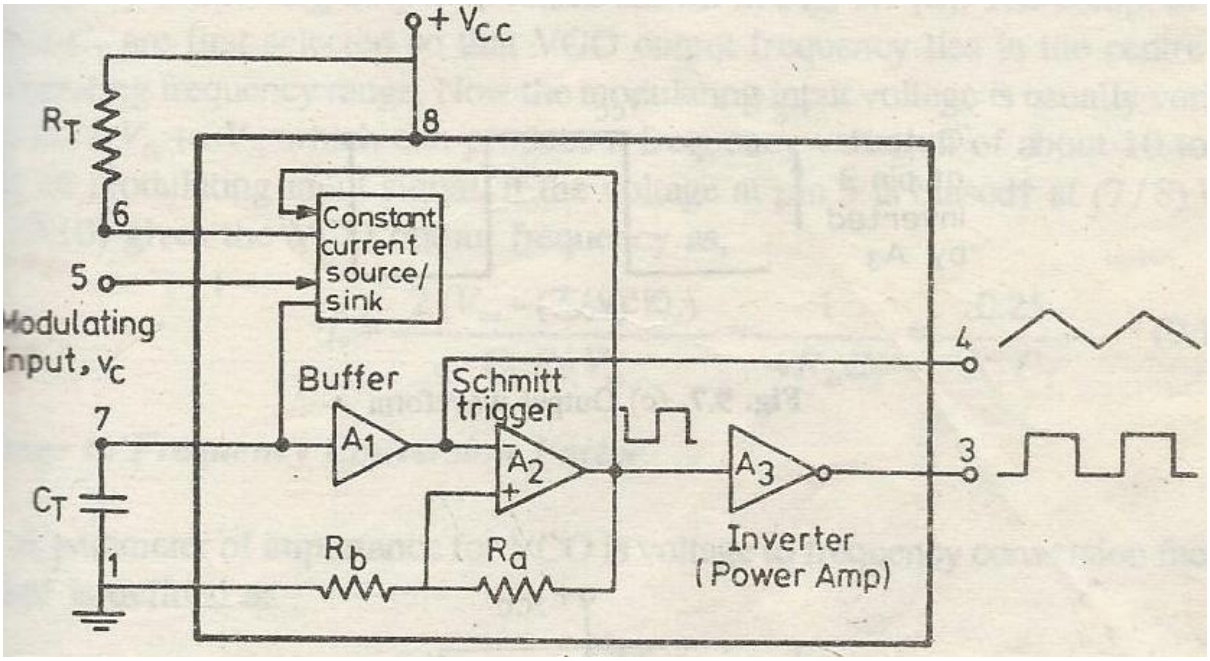


Fig (18)

This block consists of four main blocks.

i. a constant current source

ii. a buffer amplifier

iii. a Schmitt trigger

iv. an inverter

The modulating voltage also called a control voltage is applied to the modulating input (pin 5). The external capacitor charges or discharges from the constant current source. The charging current is controlled by the modulating signal or the by the external resistor Rt.

The charging voltage is decided by the Schmitt trigger. The Schmitt trigger output swings between Vcc and 0.5 Vcc. The voltage across the capacitor is applied to the buffer amplifier. If Ra = Rb, the input to the non inverting input of the Schmitt Trigger changes from 0.5 Vcc to 0.25 Vcc. When the capacitor voltage goes beyond 0.5 Vcc, the

output of the Schmitt Trigger becomes low (0.5Vcc). Now the capacitor discharges. When the capacitor voltage goes below 0.25 Vcc, the output of the Schmitt trigger becomes high (Vcc).

Because of the constant current source, the capacitor take equal timings for charging and discharging. Hence the output will be a perfect triangular one. This is available at Pin 4.

The output of the Schmitt trigger is a step voltage. So the output at Pin 3 will be a square wave.

The output frequency is given by $fo = \frac{2 (Vcc - Vc)}{CtRt (Vcc)}$

Output waveform

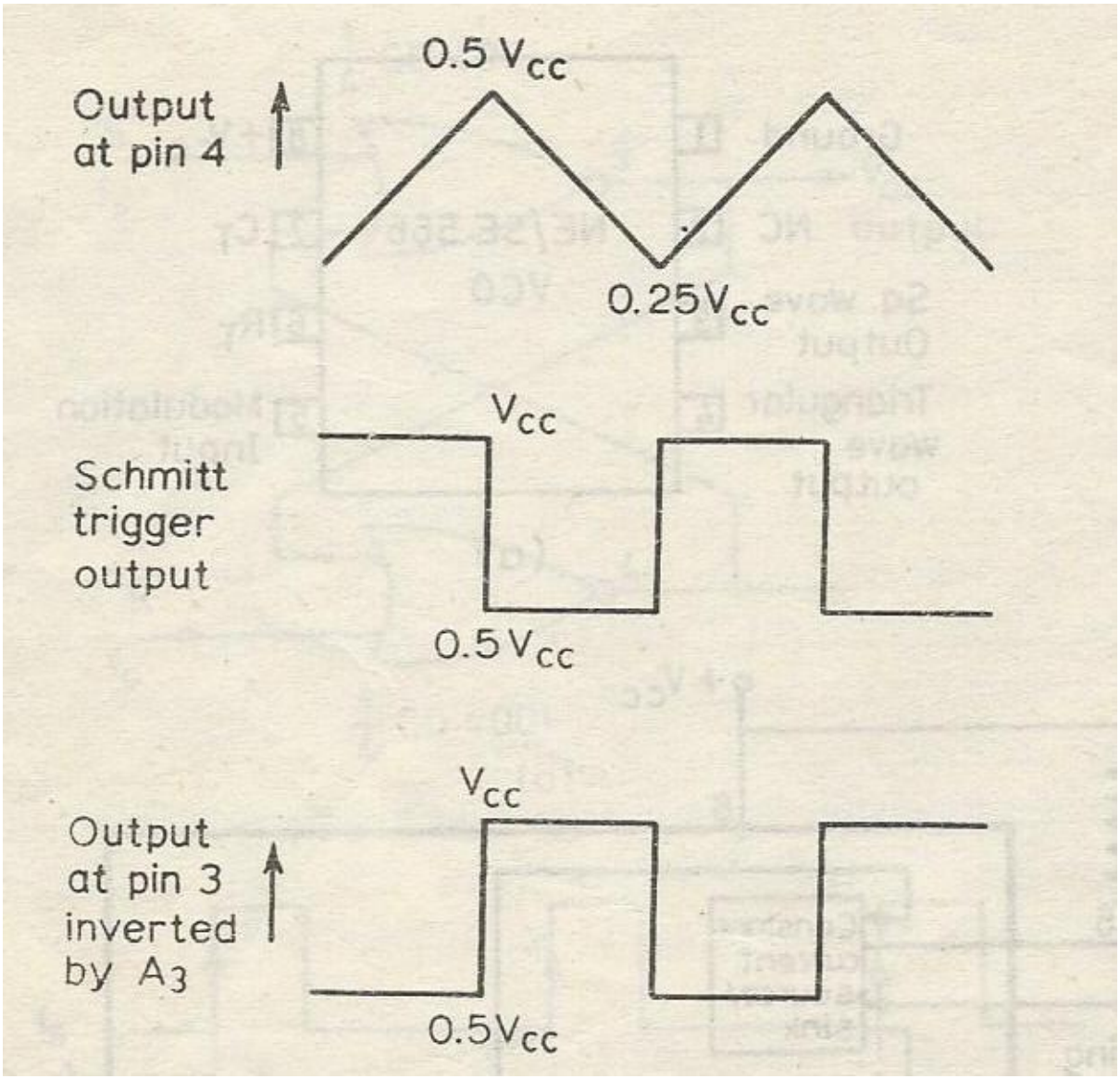
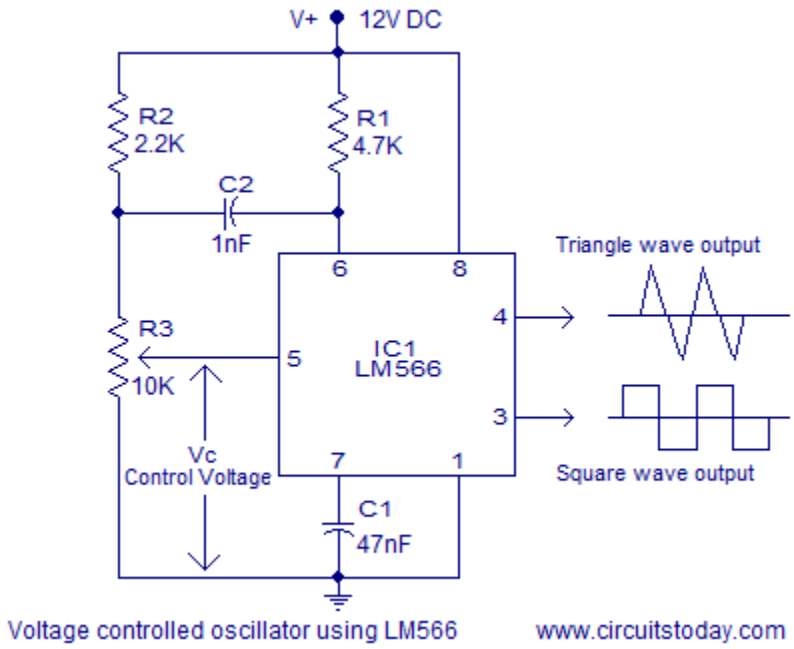


fig (19)

The LM566 IC can be operated from a single supply or dual supply. While using single supply, the supply voltage range is from 10V to 24V. The IC has a very linear modulation characteristics and has excellent thermal stability. The circuit diagram of a voltage controlled oscillator using LM566 is shown in the figure below.

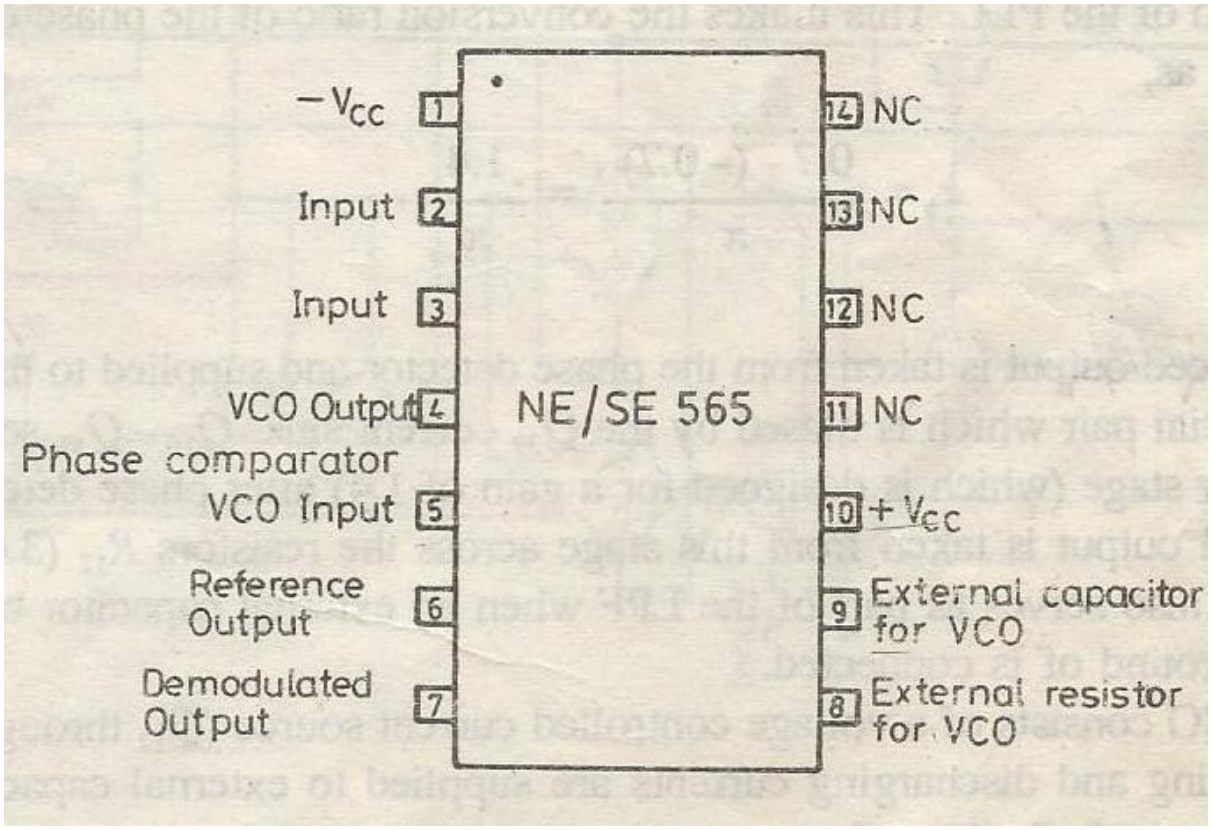


Resistor R1 and capacitor C1 forms the timing components. Capacitor C2 is used to prevent the parasitic oscillations during VCO switching. Resistor R3 is used to provide the control voltage Vc. Triangle and square wave outputs are obtained from pins 4 and 3 respectively. Output frequency of the VCO can be obtained using the following equation:

Fout = $2.4(V^+-V5)/(R1C1V^+)$. Where Fout is the output frequency, R1 and C1 are the timing components and V^+ is the supply voltage.

Monolithic PLL 565

PLL is available in different packages. Additional external components are added to the PLL to get the desired circuit. Mostly used IC is IC 565 produced by National Semiconductors.



Fig(20)

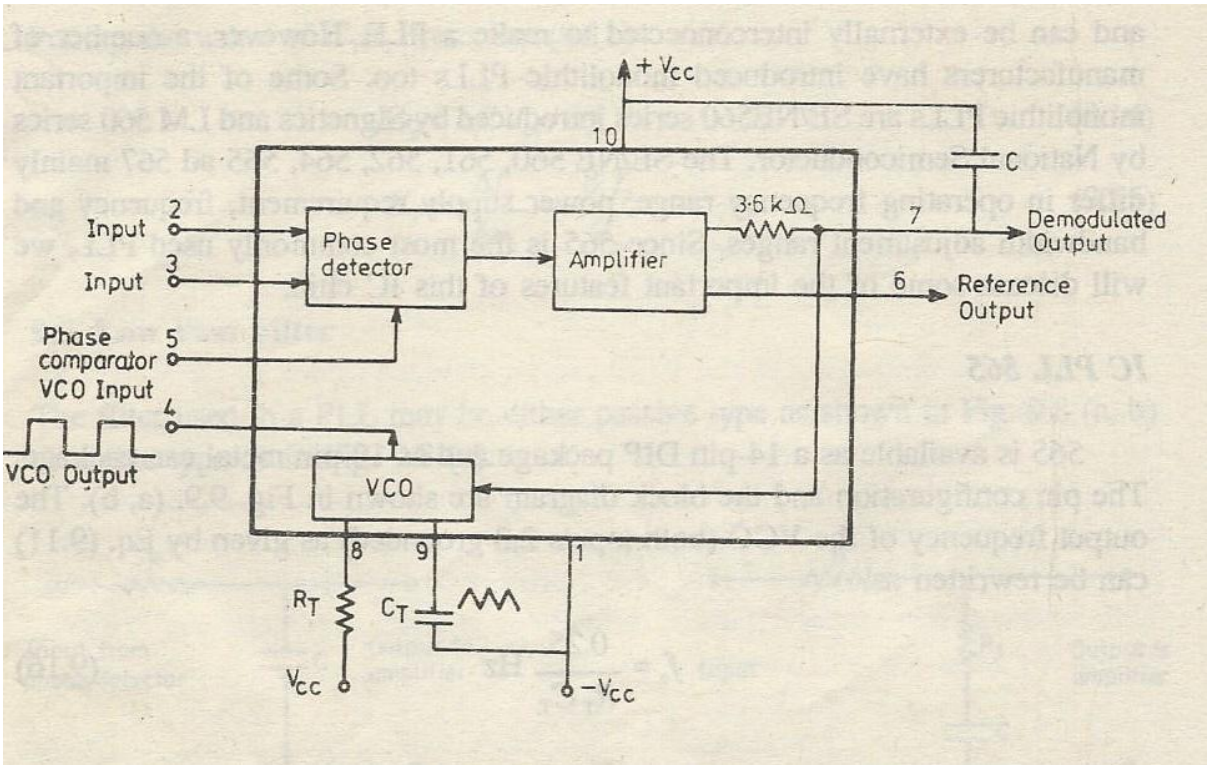
Electrical Parameter of IC 565

1. Operating frequency : 0.001Hz to 500 KHz.
2. Operating voltage range : ± 6V to ± 12 V
3. Input level : 10mV rms min to 3V pp max
4. Input impedance : 10 KΩ typical
5. Output sink current : 1 mA typical
6. Drift in VCO centre frequency with temperature : 300 ppm /ċ
7. Drift in VCO centre frequency : 1.5% / V max

With supply voltage

8. Triangle wave amplitude : 2.4 V ptp at ± 6 V supply
9. Square wave amplitude : 5.4 V ptp at ± 6 V supply
10. Bandwidth requirement : < ± 1 to > ± 60%

Functional Block Diagram of PLL 565



Fig(21)

This IC contains a phase detector, low pass filter, error amplifier and a voltage controlled oscillator. The feedback path is not closed. i.e. the output of VCO is not internally connected to the phase comparator. This may be connected to the phase comparator externally. So the VCO delivers sine wave and triangular wave as its output. The free running frequency is decided by the external resistor and capacitor. By adjusting their values the free running frequency can be changed. Generally the value of external resistor will be 2KΩ to 20KΩ where the capacitor may have any value. To control the unwanted oscillation in VCO, a capacitor Cf is connected between (pin 7) and supply voltage (pin 10)

Connection Diagram of PLL

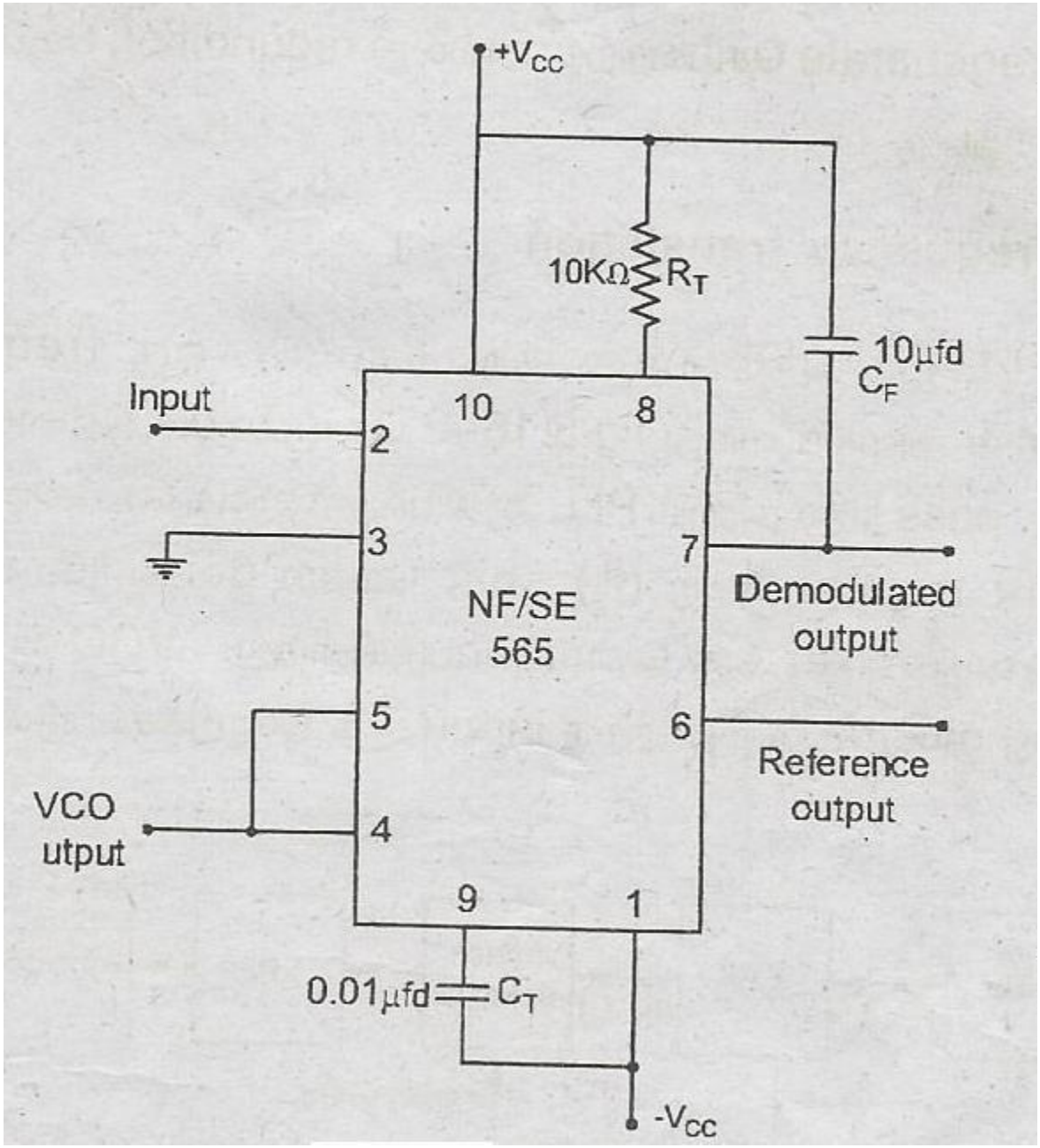


fig (22)

Frequency translation

Frequency translation is nothing but shifting the given frequency to a nearby level either in the positive or negative direction

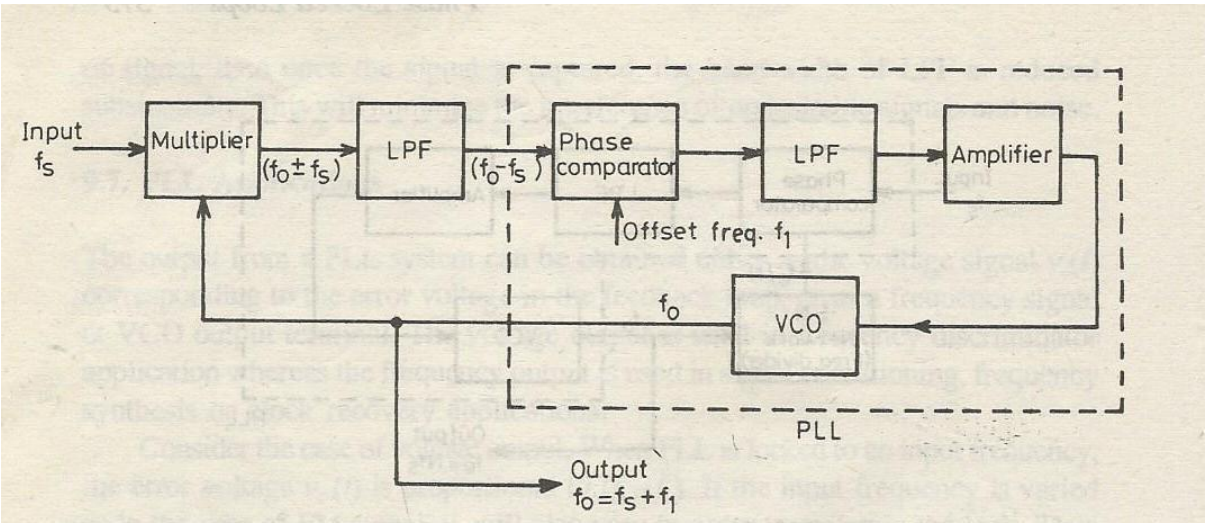


fig (23)

This circuit contains a Mixer, Low Pass Filter, Phase detector, Error Amplifier and Voltage controlled Oscillator.

The input frequency fs is to be shifted by an offset frequency fi . The input frequency fs is fed to the mixer. The other input to the mixer is the frequency fo from the voltage controlled oscillator.

The mixer mixes the two signals and produce a sum and difference frequencies (fo+fs) and (fo-fs)

These frequencies are applied to a low pass filter. This LPf allows only the low frequency (fo-fs) and filters out the high frequency (f0+fs)

The output frequency (fo – fs) of LPF is fed to a phase comparator.

The offset frequency fi (fi ‹‹ fs) is fed to the other input of the phase comparator. The phase comparator compares the two inputs and delivers an error signal.

This error signal is amplified and applied as an input to the VCO. The amplitude of this error signal decides the output frequency of the VCO.

Now the VCO is made to track the input frequency. At one point the loop is locked,

Under locked condition, the two input frequencies of Phase Comparator are equal.

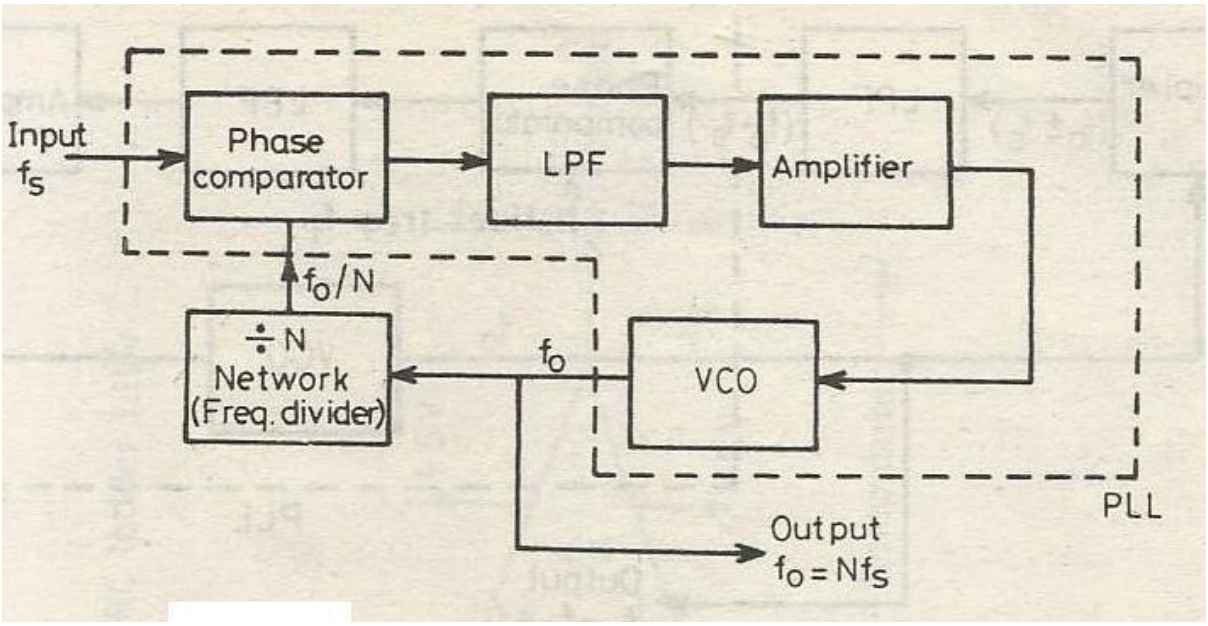
fo – fs = fi

Rearranging, fo = (fs + fi)

i.e. the input frequency fs is shifted / translated to a new value fs + fi.

Frequency Multiplication

Frequency multiplication is nothing but multiplying the given frequency with a scalar.



fig(24)

This circuit contains a Phase Comparator , Low Pass Filter, Error Amplifier and Voltage controlled Oscillator and a divide by N counter.

The input frequency fs is applied to the phase comparator. The another input to the phase comparator is the output of the counter.

The phase comprator compares the two input frequencies and delivers an error signal, This signal is amplified and fed to the Voltage controlled Oscillator.

The output frequency of the VCO depends on the amplitude of the error signal.

By adjusting the VCO, the PLL is made to lock. Under locked condition the two input frequencies of the Phase Comparator are equal

i.e. fs = fo / N

Thus, fo = N X fs.

The input frequency is multiplied by a scalar N.

By properly selecting N, any high frequency can be developed.

References

1. Linear Integrated Circuits by D. Roy Choudry and SnailJain
   Publisheers: New Age international (P) Limited, New Delhi

Review Questions

Short Answer questions

1. Define PLL.
2. Define Lock in range
3. Define capture range
4. Define Pull in time
5. Draw the pin details of IC 565
6. Draw the pin details of IC 566
7. Draw the block diagram of PLL
8. What is a phase detector? Name the types of Phase detector
9. List the applications of PLL.
10. Draw the circuit of an active LPF
11. Draw the circuit of passive LPF
12. Draw the circuit of Analog switch as phase detector.
13. Name the types of Phase comparator?

10 Mark Questions

1. Drew the block diagram of PLL and explain
2. Explain the operation of Analog Phase detector
3. Explain the operation of Balancced Modulator type Phase detector
4. Explain the operation of EX-OR phase detector.
5. Explain about the filters used in PLL
6. Give the block diagram of VCO and explain
7. How a PLL can be used as a frequency translator?
8. Draw the block diagram of PLL IC 565 and explain
9. Explain the operation of Digital phase detector
10. How a PLL can be used as a frequency multiplier?

UNIT 4: D/A AND A/D CONVERTERS

INTRODUCTION:

Naturally, physical quantities such as voltage, current, pressure & temperature signals are in analog form. It is very difficult for real time applications and to store the signals.

To solve the above problems the analog signal should be converted into digital form. It gives accuracy, speed & better performance.

In the transmitter side the analog signal has to be converted into digital form & the necessary process takes place within the computer. After completion of the process within the system, it should be again converted into the original form at the receiver side i.e., analog form. So, for a complete system Analog to Digital & Digital to Analog conversion is necessary.

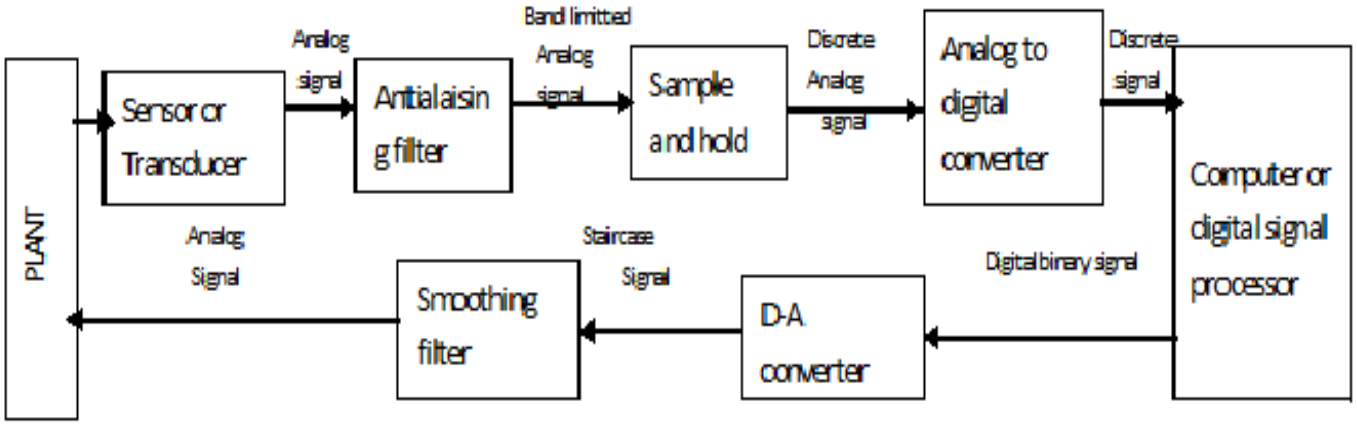
The basic building block diagram of Analog to Digital & Digital to Analog conversion is shown below:

It has 2 main parts namely,

1) Analog to Digital conversion

2) Digital to Analog conversion

BLOCK DIAGRAMOF ADC & DAC



1) Analog to Digital conversion:

The sensor & transducer connects the input analog signal to the Analog to Digital converter & it converts the non electrical input signal into electrical signal.

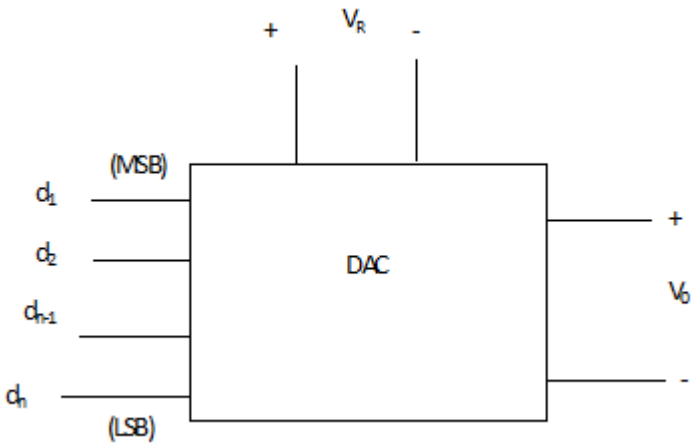
Antialiasing filter is used to band limit the analog signal i.e., there by band width requirement is reduced. Sample & hold circuit is used to sample the band limited signal based on the sample theorem. So the signal becomes a discretized signal. Though the signal is in analog form, hold the discrete signal until the conversion is completed.

Analog to Digital converter converts the discretized signal into binary digits i.e., discrete digital signal and then it is given to the processors.

2) Digital to Analog conversion:

Digital to Analog conversion is just the reverse process of Analog to Digital conversion.

BASIC STRUCTURE OF DAC



It has i) Digital to Analog converter

ii) Smoothing filter.

Digital to Analog converter is used to convert the digital binary bits into analog signal. But Analog to Digital converter & Digital to Analog converters are operated at same frequency.

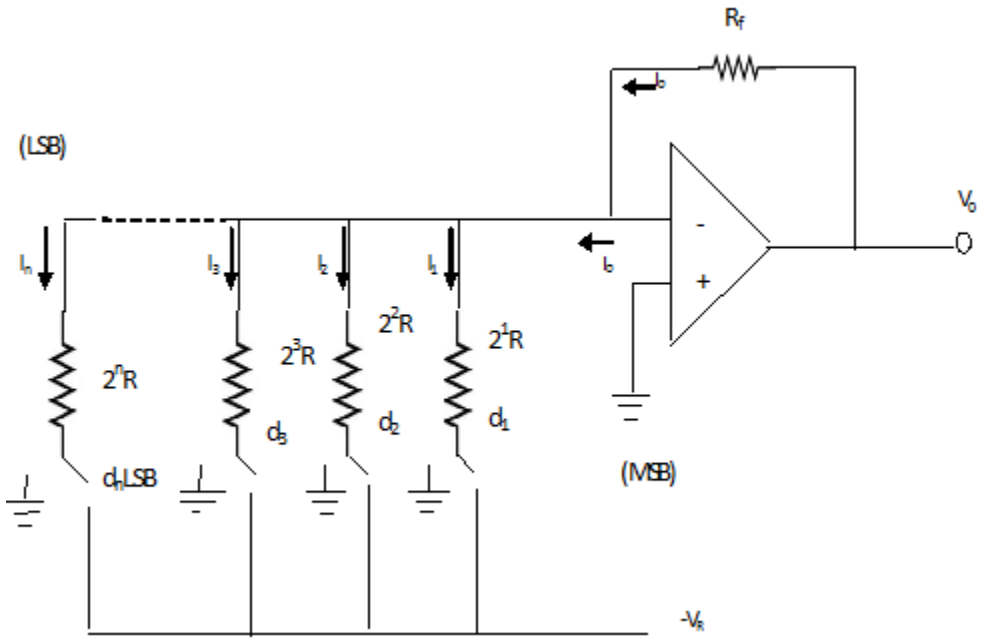
The Digital to Analog converter produces a staircase output & which is given to the smoothing filter. The smoothing filter is used to convert the stair case signal to the smooth analog signal. Also the smoothing filter reduces the quantization noise. Analog to Digital & Digital to Analog converter is designed in same circuit i.e., a circuit that can act as an Analog to Digital & Digital to Analog converter is called Data converter & it is also available in the form of integrated chip IC.

TYPES OF DAC

1. Weighted resister

2. R-2R ladder network

WEIGHTED RESISTOR:



It consists of: i) Summing amplifier

ii) Different ranges of resistor

iii) Electronic switches.

All the resistors are connected as network & the network is connected with summing amplifier. Each resistor is connected with its own switch. The electronic

switch is used to connect & disconnect the corresponding resistor with the network and also its input binary bits.

The switch can be connected to two positions

i) Input ii) Ground

If the switch is connected with the input there is a voltage drop across the resistors. If input is zero then the switch is connected with ground. If the output current I_0 can also be written as:

$$I_0 = I_1 = I_2 + I_3 + \ldots\ldots\ldots + I_n$$

$$I_Q = \frac{V_R\, d_1}{2^1 R} + \frac{V_R\, d_2}{2^2 R} + \ldots\ldots\ldots \frac{V_R\, d_n}{2^n R}$$

Disadvantages:

1) Wide range of resistors is needed.

2) If number of bits increases, then number of resistors and switches also increases.

3) If the word length increases, then the circuit becomes complex.

$$I_0 = \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots\ldots + d_n 2^{-n}\right)$$

We know that $V_0 = I_0 R_f$

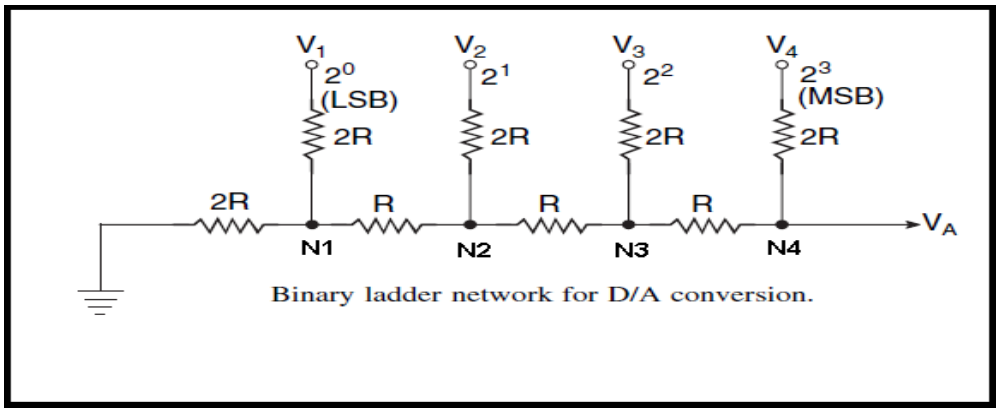
$$I_0 = \frac{V_R}{R} R_f (d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n})$$

If $R_f = R$

$$V_0 = V_R (d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n})$$

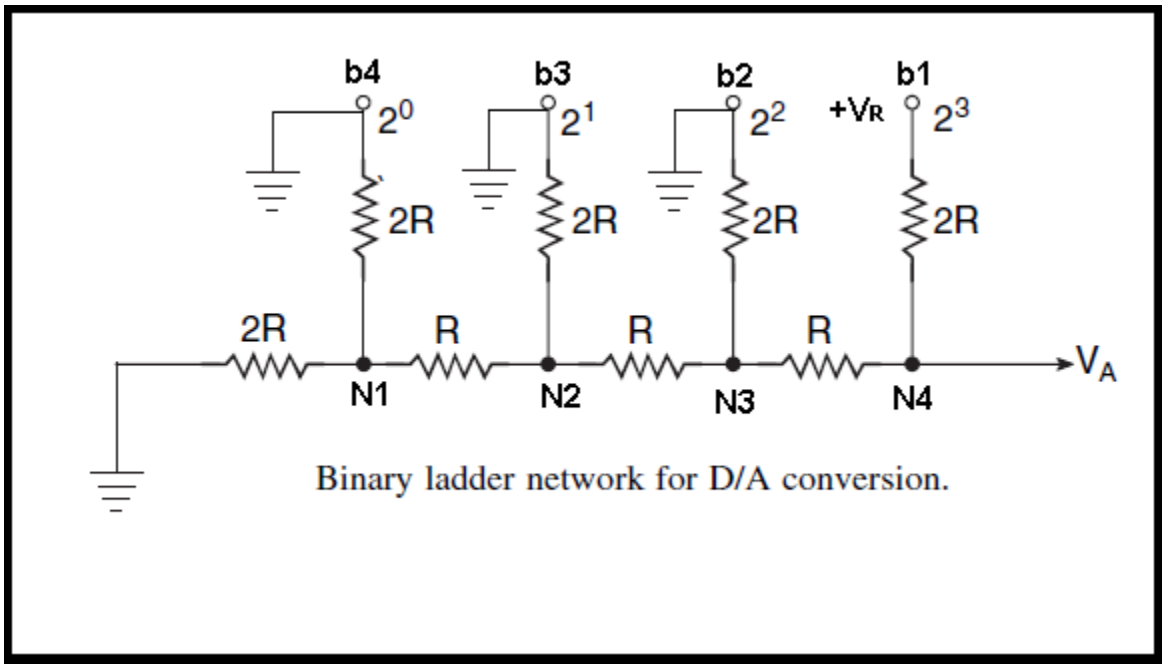
R-2R LADDER DAC:

To overcome huge range of resistor used in weighted resistor D/A converter, R-2R ladder D/A converter is introduced. In my previous post I discussed about weighted resistor D/A converter. But the vital problem in weighted register D/A converter is use of huge range of different resistance. Suppose we have to design 8-bit weighted register D/A converter then we need the resistance value $2^0R+2^1R+\ldots.+2^7R$. So the largest resistor corresponding to bit b_8 is 128 times the value of the smallest resistor correspond to b_1. But in case of R-2R ladder D/A converter, Resistors of only two values (R and 2R) are used. Now in bellow see the simple ladder network.



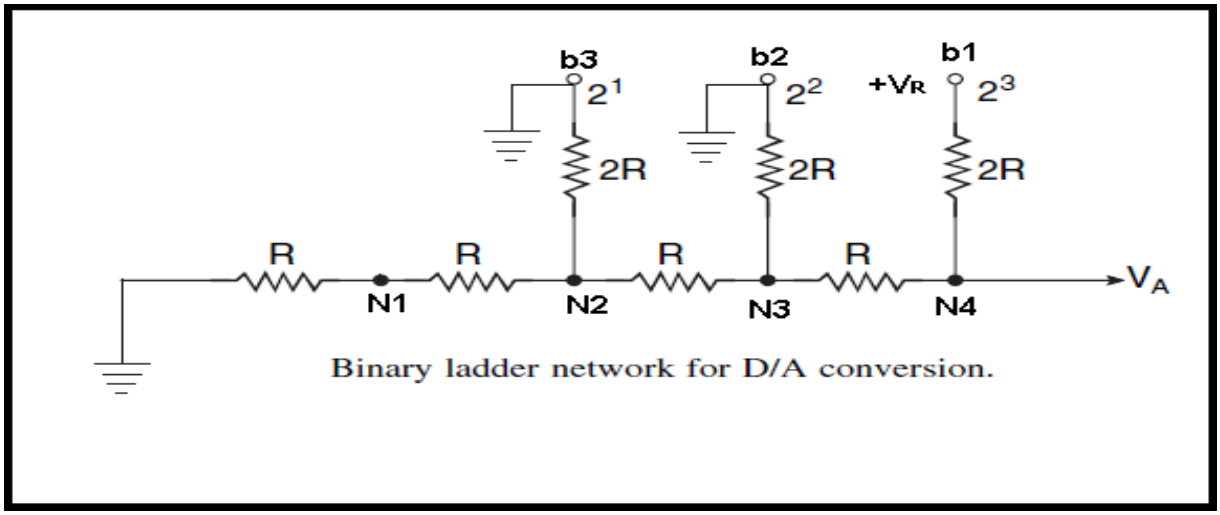
Binary ladder network for D/A conversion.

In ladder circuit the output voltage is also weighted sum of the corresponding digital input. Let us take an example to understand how it works. As we can see the above network is a 4-bit ladder network, so let us take an example to convert analog signal correspond of 1000 digital bit. For 1000 bit we can see only MSB got 1 and rest all bits got 0. See the bellow picture to understand how it work if it got 1000.



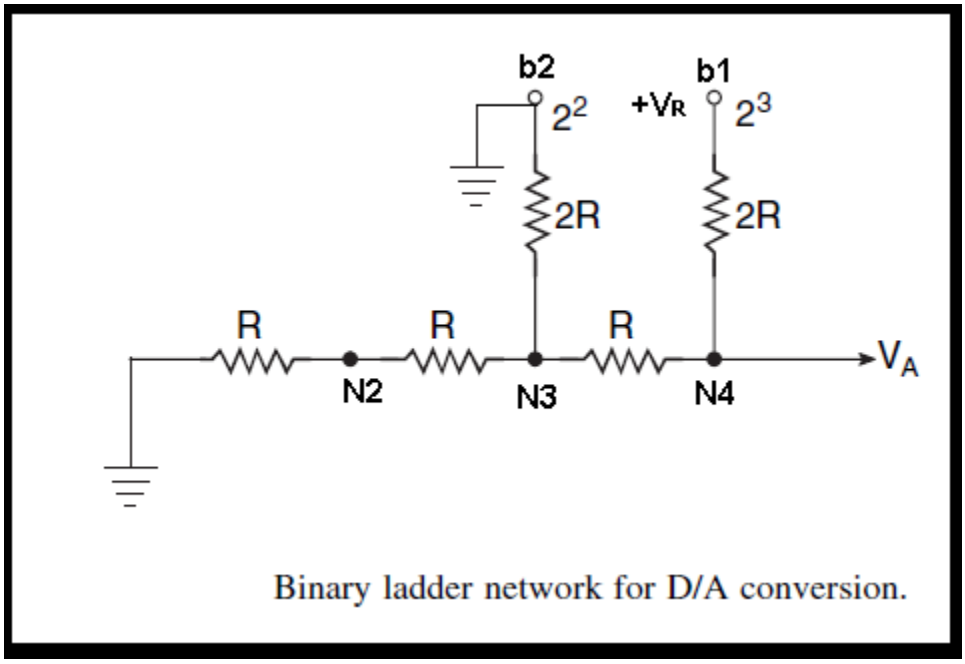
Binary ladder network for D/A conversion.

Now see at node1 (N1) resistor 2R connecting in b4 parallel with resistor 2R. And those 2R parallel 2R resistors make equivalent register of R shown in bellow diagram.



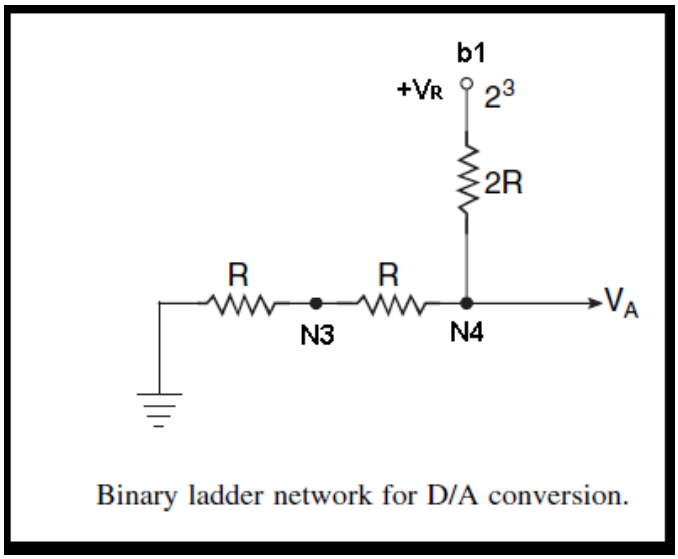
Binary ladder network for D/A conversion.

Now for N2 same thing happen B3 series with 2R and parallel with R + R resistors. It will also make equivalent resistor R at N3. See the bellow diagram



Binary ladder network for D/A conversion.

Repeating the same process we got equivalent of R resistor at N4.



Binary ladder network for D/A conversion.

Now at N4, if we calculate the output analog equivalent voltage then we will get

$$V_A = V_R*2R/(R+R+2R)$$

$$= V_R/2$$

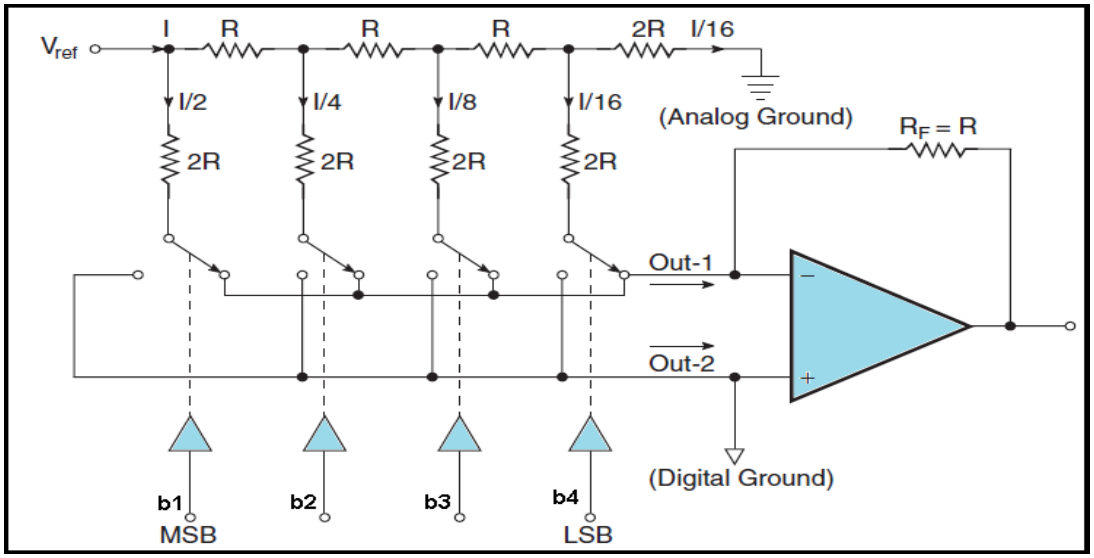
Thus when bit 1000 the output is $V_R/2$. Similarly it can be found that using above process for bit 0100 the output will be $V_R/4$, for bit 0010 outputs will be VR/8 and for bit 0001 output will be VR/16.

By using superposition theorem we can find in any n-bit ladder network the output voltage will be

$$V_A = V_R/2^1 + V_R/2^2 + V_R/2^3 + \ldots\ldots + V_R/2^n$$

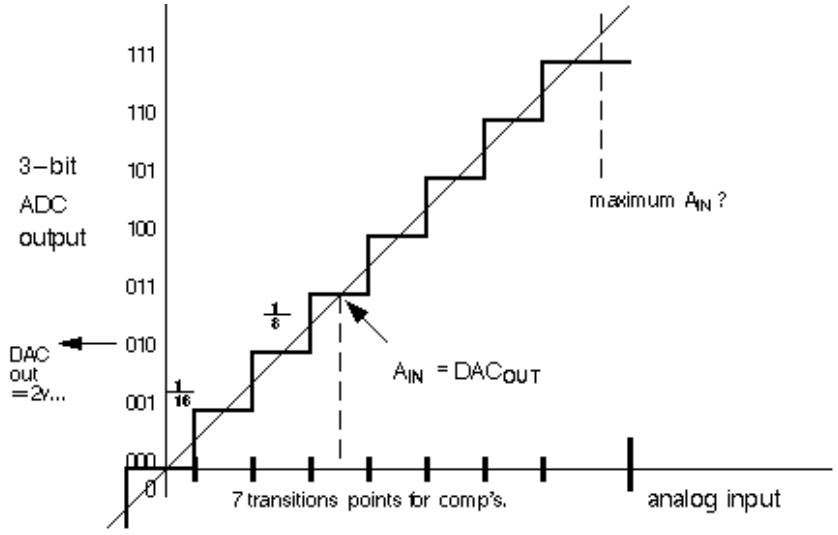
Where n is the total number of bits at the input.

Now see the practical circuit arrangement of 4-bit R-2R ladder D/A converter using op amp.



The inverting input terminal of the op amp work as a summing amplifier for the ladder inputs. So we can get out put voltage by bellow equation.

$$\mathbf{V0 = V_R*(R_F/R)[b1/2^1 + b2/2^2 + b3/2^3 + b4/2^4]}$$



SPECIFICATIONS OF DAC:

Specifications of DAC are

1. Accuracy

2. Resolution

3. Monotonocity

4. Settling time.

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

Resolution:

It can also be defined as the ratio of change in analog output voltage resulting from a change of 1LSB at the digital input. For n-bit DAC,

Resolution=$V_{FS}\,(2n-1)$

Resolution should be high as possible. It depends on the number of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution.

Monotonocity:

In an ideal D/A converter, the analogue output should increase by an identical step size for every one-LSB increment in the digital input word or A D/A converter is considered as monotonic if its analogue output either increases or remains the same but does not decrease as the digital input code advances in one-LSB steps.

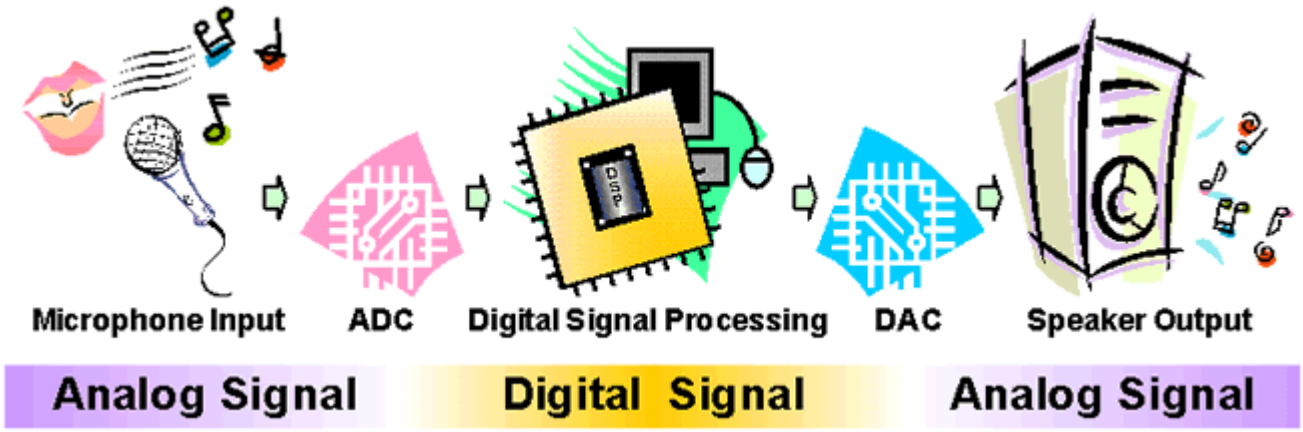
Settling time:

The *settling time* is the time period that has elapsed for the analogue output to reach its final value within a specified error band after a digital input code change has been effected. General-purpose D/A converters have a settling time of several microseconds, while some of the high-speed D/A converters have a settling time of a few nanoseconds.

BASICS OF A-D CONVERSION

In modern life, electronic equipment is frequently used in different fields such as communication, transportation, entertainment, etc. Analog to Digital Converter

(ADC) and Digital to Analog Converter (DAC) are very important components in electronic equipment. Since most real world signals are analog, these two converting interfaces are necessary to allow digital electronic equipments to process the analog signals.



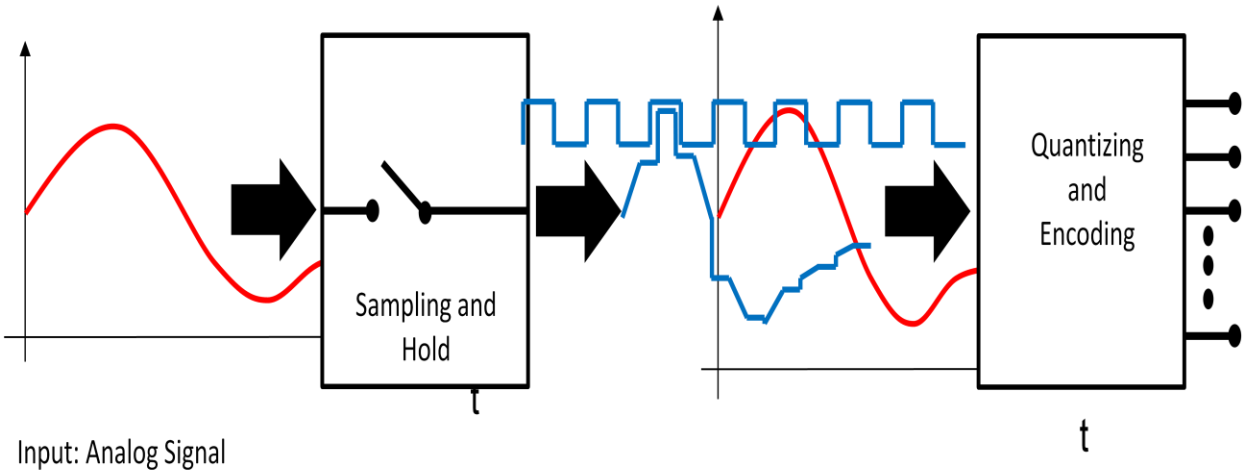
In electronics, an Analog to Digital Converter (ADC) is a device for converting an analog signal (voltage, current etc.) to a digital code, usually binary. In the real world, most of the signals sensed and processed by humans are analog signals. Analog to Digital conversion is the primary means by which analog signal are converted into digital data that can be processed by computers for various purposes.

In A/D conversion, there are two main steps of process:

1. Sampling and Holding

2. Quantization

In order to be able to perform digital signal processing on natural signals that are analog in nature, they must first be sampled and quantized into digital form.



TYPES OF **A** to **D** CONVERTOR:

1) Direct type

i) Flash type

ii) Successive Approximation

2) Integrating type of ADC

i) Dual slope ADC

ii) Ramp type

DIRECT TYPE

i) FLASH TYPE:

It is one of the simplest types of ADC. In the above diagram resistors are connected in network and it acts as a voltage divider. The resistive network is

connected with the comparator. The comparator itself can resolve the problem while it is given with the same level of voltage.

Generally the comparator compares the 2 levels of voltages given to its 2 input terminal. If he analog input voltage V_a is connected with the non inverting terminal and the reference voltage V_r is given to its inverting terminal.

The comparator compares these 2 voltages (V_a & V_r) and produces its output as:

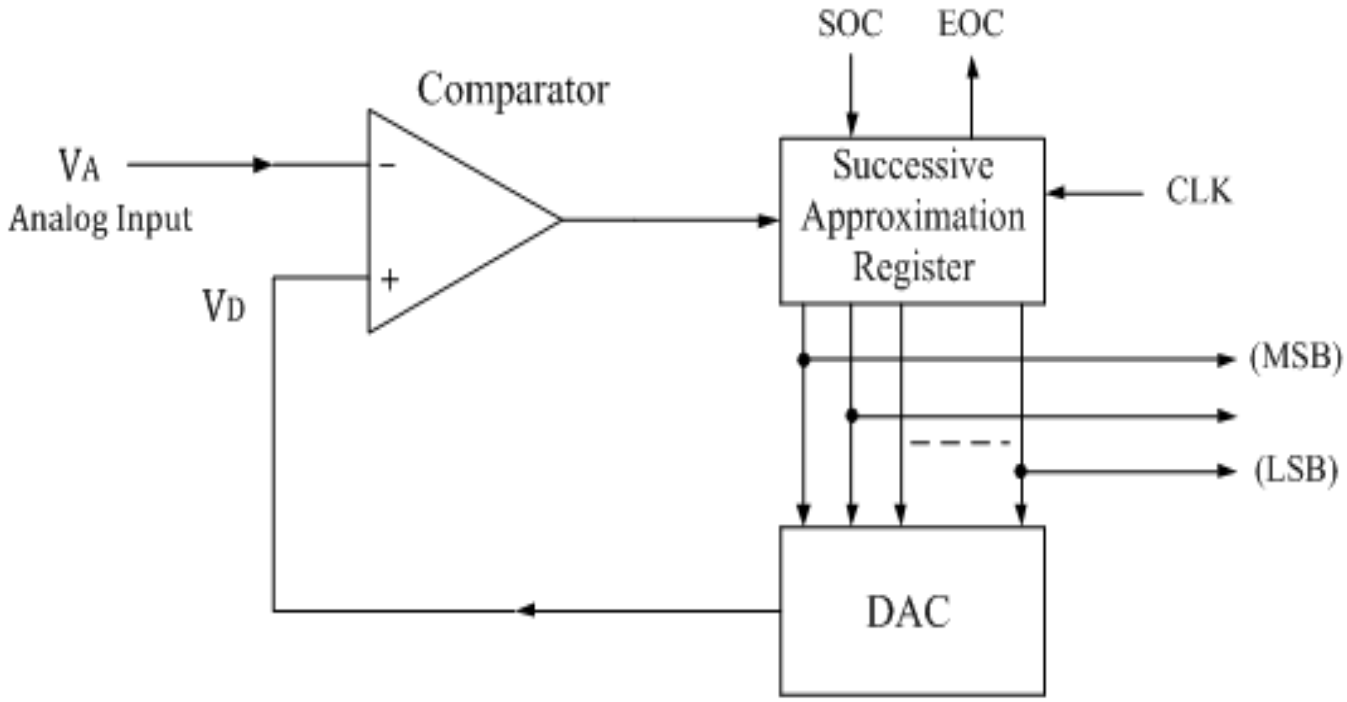
i) If V_a greater than V_d output will be 1.

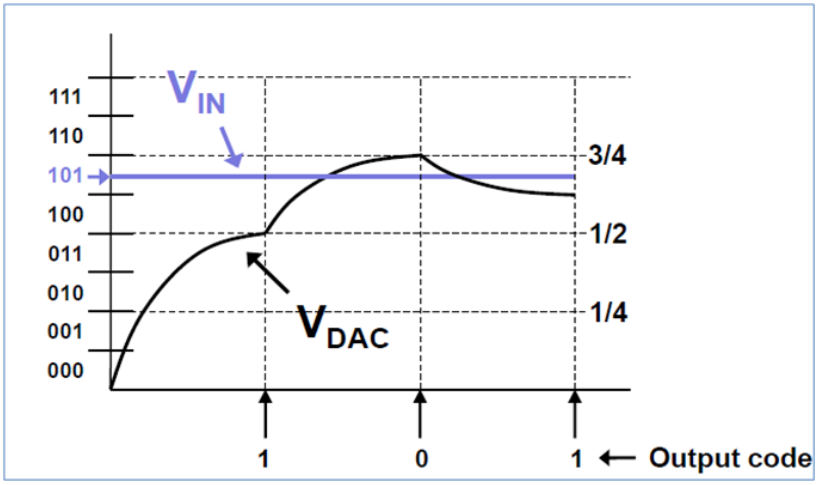
ii) If V_a greater than V_r output will be 0.

iii) If $V_a = V_d$ the previous value will be maintained.

This comparison takes place simultaneously at all the nodes within 100ns. The conversion speed is depends upon the comparator speed and the priority encoder. The main drawback of this convertor is that it requires more number of comparator for minimum number of bit operations. That is for 'n' number of bits conversion it needs 2^nn-1 number of comparator. It will increase the cost of the system.

ii) SUCCESSIVE APPROXIMATION CONVERTER





It is one of the efficient methods of ADC. It needs ‘n’ number of clock periods for ‘n’ number of bits conversion.

The above block diagram consists of 3 main parts:

i) Comparator

ii) Successive Approximation registers

iii) DAC

The analog input voltage V_a is given to the inverting terminal of comparator and the output of DAC is given to the non inverting terminal of the comparator.

If the start pulse is given to SAR, the SAR makes d_1 become one state and makes all other bits are to be zero, so that the code of SAR is 100000000. The output of DAC called V_d is compared with V_a is greater than V_d then the code generated is less than the digital representation.

Then consider the next MSB bit & make it to 'I'. So the data bit becomes 01000000 & it is also tested further and so on. However if $V_a < V_d$ then the data bit is greater than the correct digital representation. At the time the SAR reset the MSB to zero & make the next lower MSB to be 'I' and it will be continuous process until all the bits are tested correctly.

After finishing the conversion is given to SAR to reset the SAR to start the next code word operations.

INTEGRATING TYPES

i) DUAL SLOPE ADC: There are 3 main parts are available. They are

i) Buffer amplifier

ii) Integrator

iii) Voltage comparator.

It consists of A_1 buffer with high input impedance. The analog input voltage is given to the integrator A_2 through the buffer A_1.

The integrator integrates the analog signal with a time period 2^n with respect to the reference voltage V_R. This process of integration will go on until the integrator output becomes 0. The 'N' number of clock pulses is required to make the integrator output 0.

Before START command is given, the switch SW_1 is grounded and SW_2 is closed. After integration the offset voltage in AmplifierA_1, AmplifierA_2 and comparator loop can be seen across the capacitor C_{AZ}.

Here the capacitor C_{AZ} provides the offset voltages for all the op-amp.

When SW_2 is open, then C_{AZ} act as a memory to keep the offset voltage. When the 'start' command is given to control logic at a time $t=t_1$, the SW_2 opens and SW_1 closed. So V_a is passed. So the counter starts to count.

Here $T_1 = 2^n \times T$

Where T_1=Tune taken to reset the counter to 0

2^n=No. of clock pulses.

T = clock period.

After resetting of the counter, the SW is connected to the reference voltage $-V_R$.

So the output voltage V_0 have +ve slope. If V_0 is –ve then the comparator output is +ve. So the counter stars to count.

When V_0 is 0 at $t=t_3$ EOC activated from the slope.

$T_1 = t_2 - t_1 = 2^n$ counts

Clock rate

$t_3 - t_2 = \frac{\text{digital count N}}{\text{Clock rate}}$

$\Delta V_0 = \left[\frac{-1}{RC}\right] V(\Delta t)$

From the slope

At t_2 $V_0 = V_2$

Then $V_1 = \left[\frac{-1}{RC}\right] V_a (t_2 - t_1)$

V_1 can also be written as

$V_1 = \left[\frac{-1}{RC}\right] (-V_R)(t_2 - t_3)$

$V_1 = V_a(t_2 - t_1) = V_R(t_3 - t_2)$

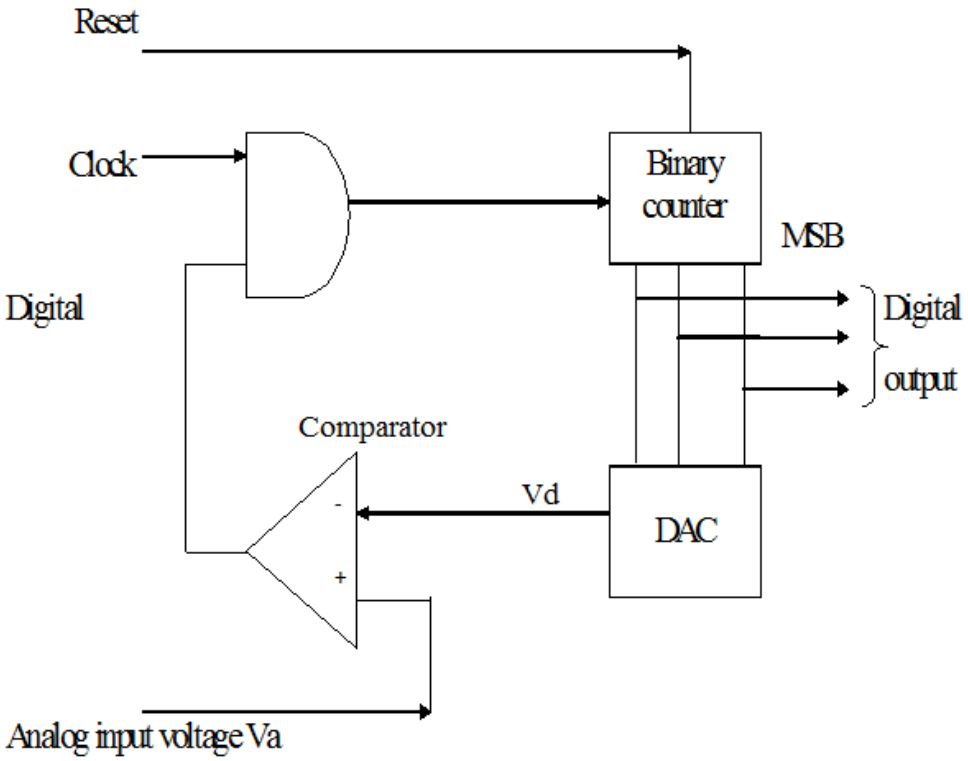
$(t_2 - t_1) = 2^n$ & $(t_3 - t_2) = N$

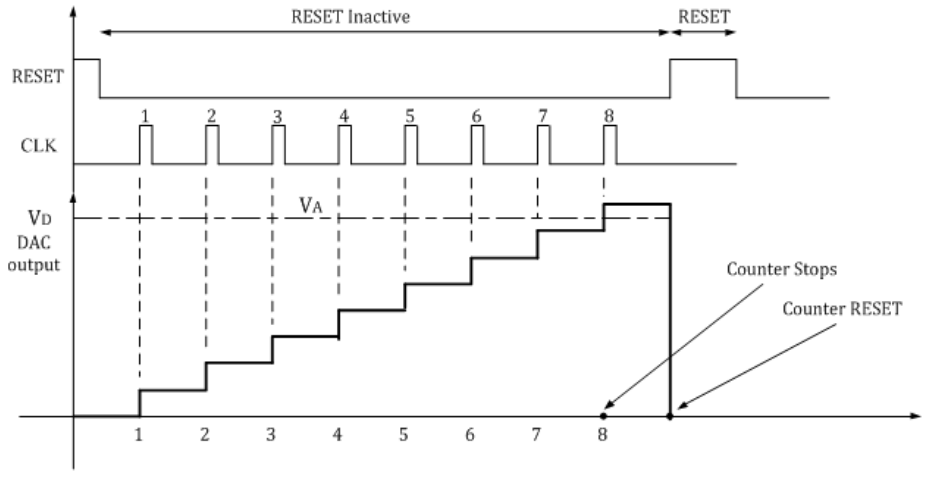
$V_1 = V_a(2^n) = V_R N$

$V_a = V_R \left[\frac{N}{2^n}\right]$

The main disadvantage of dual slope ADC is long conversion time. But it is very accurate for slowly varying signal conversions.

ii) RAMP TYPE





The reverse operation of DAC is ADC with this concept the above type of ADC is designed.

Before starting the operation we have to reset the counter to zero to clear the data which was already stored in the counter register. After the applying the reset the number of clock pluses are counted by the binary counter. When the comparator produces high signal at its output it drives the Gate then the gate produces pulses to the binary counter and the counter will count the number of pulses which are received. If the time is increased, the number of pulses are also be increased and it will leads to increase the counter value.

The comparator is used to compare Va and Vd and according to these voltage levels it can produce low or high levels at its output.

If Va > Vd , the output of the comparator will be high and the AND gate will be enabled.

If Va < Vd , the output of the comparator will be low and the AND gate will be disabled.

If Va <= Vd , at the time the comparator drives the to produce zero value to the counter and the counter releases its count number. That number is equal to Va.

The main drawback of this type of counter is the counter frequency must be low enough to give

THE INTERNAL BLOCK DIAGRAM OF ADC0809/ADC0808 IC,

The various functional blocks of ADC are 8-channel multiplexer, comparator, 256R resistor ladder, switch tree, successive approximation register, output buffer, address latch and decoder.

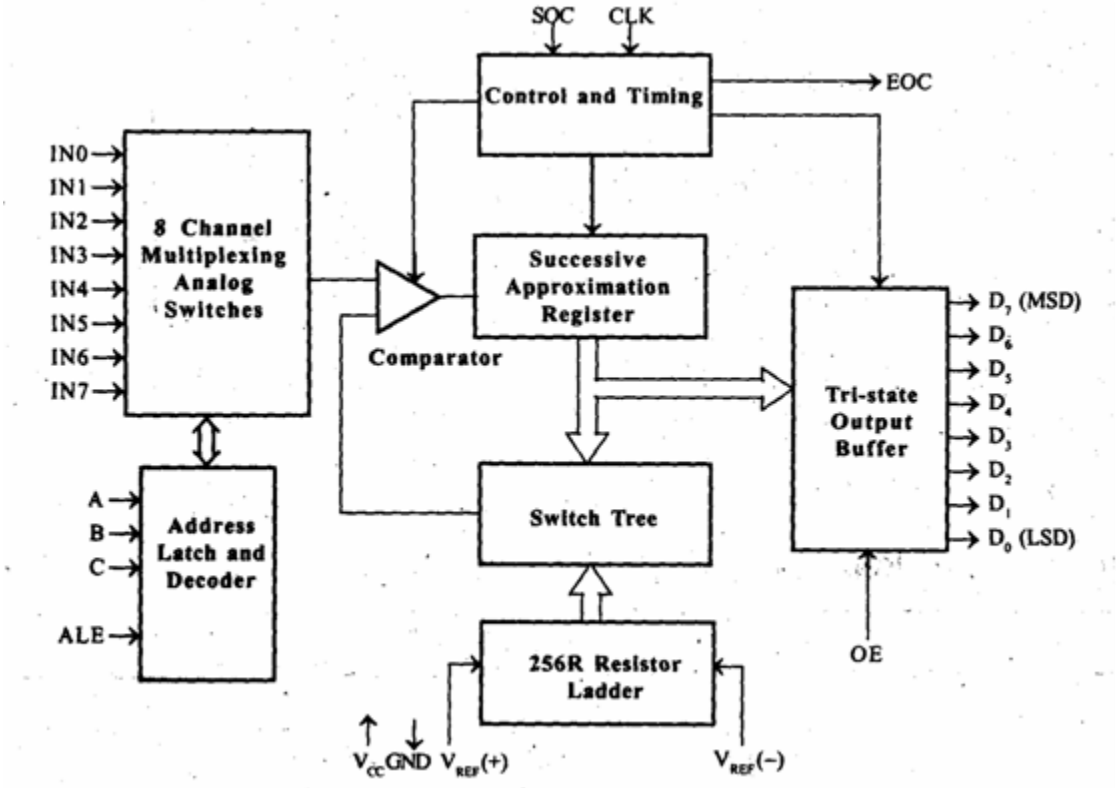
- The 8-channel multiplexer can accept eight analog inputs in the range of 0 to 5V and allow one by one for conversion depending on the 3-bit address input. The channel selection logic is,

Address Input			Selected Channel
C	B	A	
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

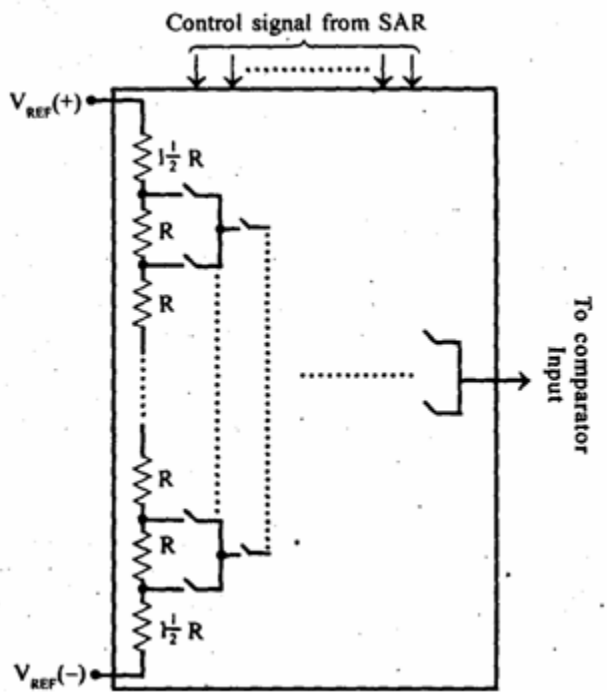
- The successive approximation register (SAR) performs eight iterations to determine the digital code for input value. The SAR is reset on the positive edge of START pulse and start the conversion process on the falling edge of START pulse.

A conversion process will be interrupted on receipt of new START pulse.

The End-Of-Conversion (EOC) will go low between 0 and 8 clock pulses after the positive edge of START pulse.
The ADC can be used in continuous conversion mode by tying the EOC output to START input. In this mode an external START pulse should be applied whenever power is switched ON.



- The 256'R resistor network and the switch tree is shown in fig.



- The 256R ladder network has been provided instead of conventional R/2R ladder because of its inherent monotonic, which guarantees no missing digital codes.

- Also the 256R resistor network does not cause load variations on the reference voltage.

- The comparator in ADC0809/ADC0808 is a chopper- stabilized comparator. It converts the DC input signal into an AC signal, and amplifies the AC sign using high gain AC amplifier. Then it converts AC signal to DC signal. This technique limits the drift component of the amplifier, because the drift is a DC component and it is not amplified/passed by the AC amp1ifier. This makes the ADC extremely insensitive to temperature, long term drift and input offset errors.

- In ADC conversion process the input analog value is quantized and each quantized analog value will have a unique binary equivalent.

- The quantization step in ADC0809/ADC0808 is given by,

$$Q_{step} = \frac{V_{REF}}{2^8} = \frac{V_{REF}(+) - V_{REF}(-)}{256_{10}}$$

The digital data corresponding to an analog input (V_{in}) is given by,

$$\text{Digital data} = \left(\frac{V_{in}}{Q_{step}} - 1\right)_{10}$$

x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x-x

UNIT 5: SPECIAL FUNCTION ICs

INTRODUCTION

The 555 timer IC was introduced in the year 1970 by Signetic Corporation and gave the name **SE/NE 555 timer**. It is one of the monolithic timing circuits and important use of this IC is providing accurate and constant delay to the circuit. And the other advantages of this IC are very compact size, more reliable, and low cost also. IC555 are very much used in different fields. Some of the applications are given below.

Applications of IC555 are

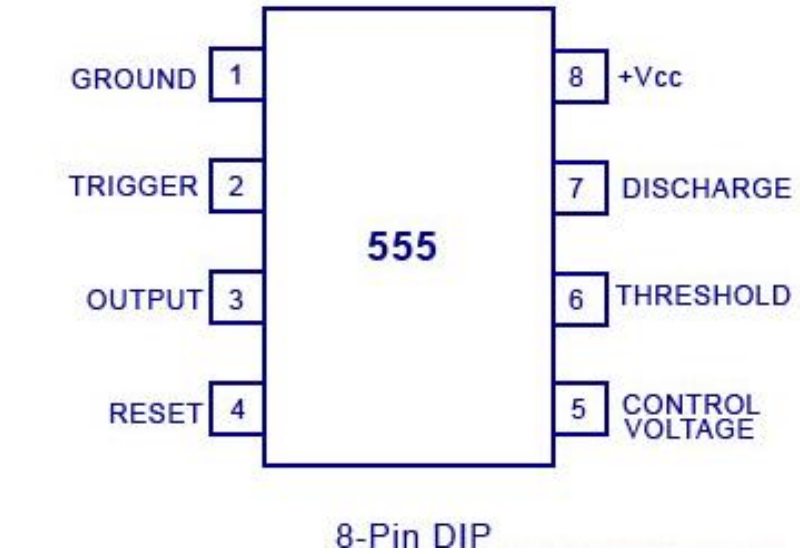
1.Monostable multivibrator

2. Astable multivibrator

3. Wave form generators

4. DC-DC convertor etc.

PIN DIAGRAM OF IC 555



8-Pin DIP

Pin descripion:

Pin 1: **Grounded Terminal:** The given input voltages and output voltages are measured with respect to ground.

Pin 2: Trigger Terminal: The trigger voltage defines the output of the timer.

Pin 3: Output Terminal: Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the *normally on load* and that connected between output and ground pin is called the ***normally off load***.

Pin 4: Reset Terminal: It is used to reset the timer .By applying high signal to the terminal it can reset the timer.

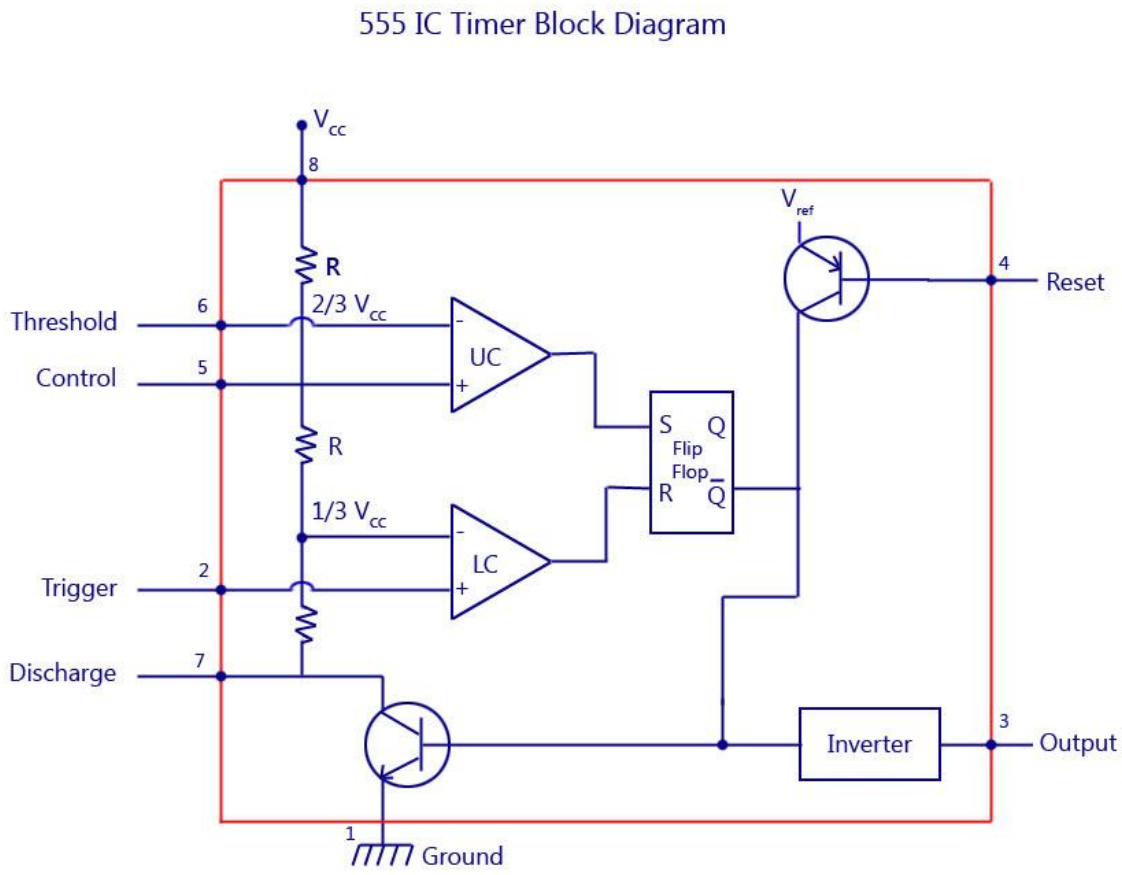
Pin 5: Control Voltage Terminal: The amount of control voltage controls the width of the output pulses.

Pin 6: **Threshold Terminal:** This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. If the applied voltage crosses the threshold level then the upper comparator output becomes high and the output goes to low.

Pin 7 : **Discharge Terminal:** This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

Pin 8: Supply Terminal: the supply voltage range of the IC can be +5v to +18v.

FUNCTIONAL DIAGRAM OF 555 IC



WORKING PRINCIPLE

The above block diagram consists of upper and lower comparators , flip flops, invertors ,amplifier and resistive network.

The resistive network connected here are act as a voltage divider which divides the Vcc into 2 levels, one level is 2/3Vcc and one more level is 1/3Vcc. 2/3 Vcc is given to the inverting terminal of upper comparator it is it's threshold level and (1/3)Vcc at the inverting terminal of the lower comparator. The upper and lower comparator are used to set and reset the flip flop and also these 2 comparators are the responsible for charging and discharging the transistor Q1 and Q2 .The upper comparator has the reference level of 2/3 Vcc and the lower comparator has the reference level of 1/3Vcc.In general The threshold voltage and trigger voltage can control the timer , so there is no need of special control voltage given to it. If we

want to change the width of the pulse ,we have to give control voltage separately at pin 5.

When the trigger voltage applied,

When the trigger voltage is applied to the inverting terminal of the comparator C2 through 1/3Vcc at its noninverting terminal, the comparator changes the state of flipflop to set state. Then the output of flip-flop makes the transistor to low level.

When the threshold voltage applied,

When the threshold voltage is applied to the comparator C1 through the reference voltage of 2/3 Vcc, the output of the comparator will also change the state of flipflop to reset. Then the transistor acts as a buffer.

APPLICATIONS OF 555IC

applications as a

1.M**onostable multivibrator**

2. **Astable multivibrator**,

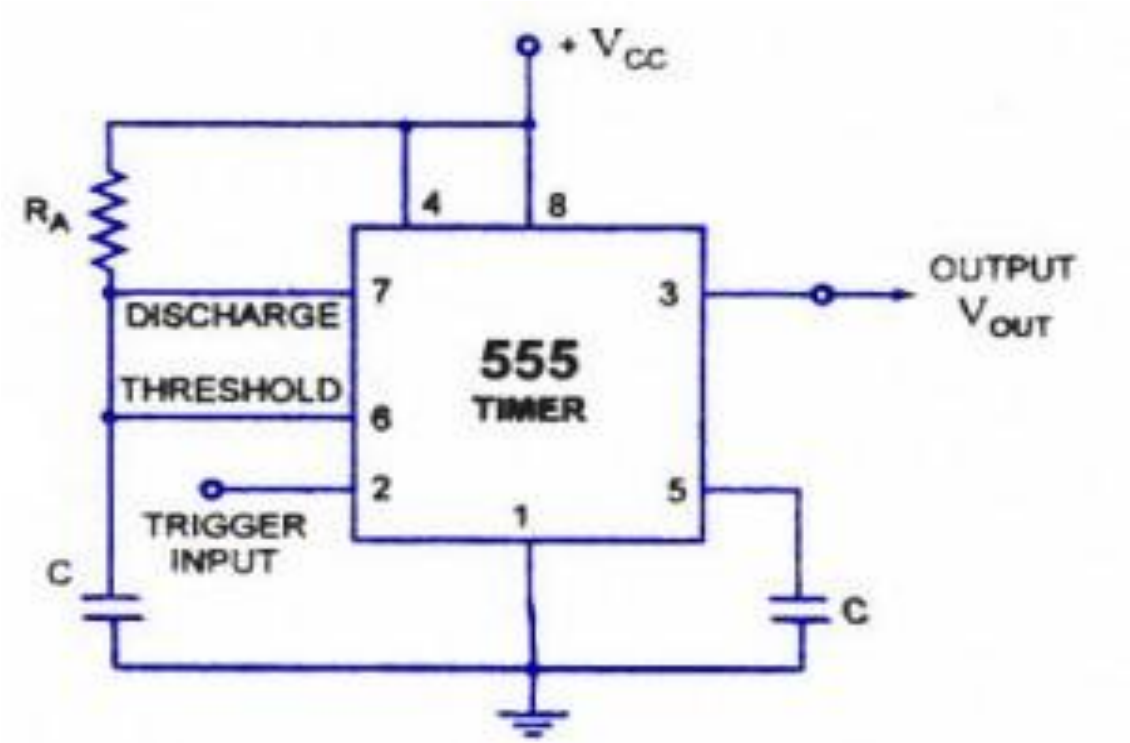
3. Schmitt trigger

4. **Dc-dc converters**

5. **Waveform generators**

6. **Temperature measurement** and etc.,

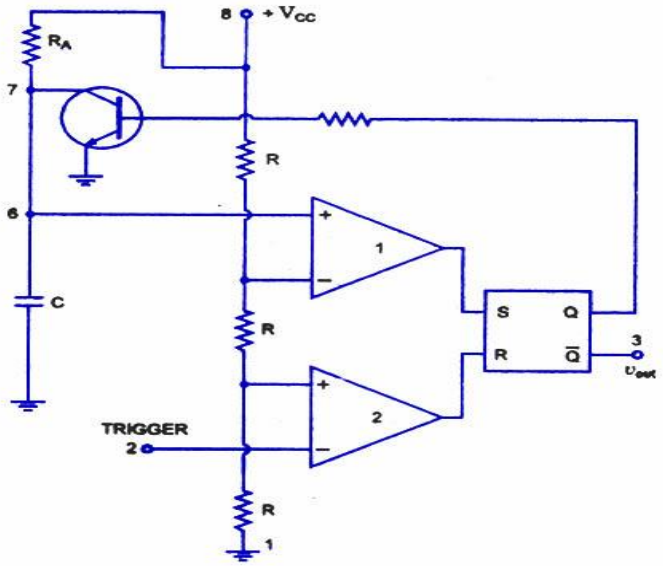
MONOSTABLE MULTIVIBRATOR



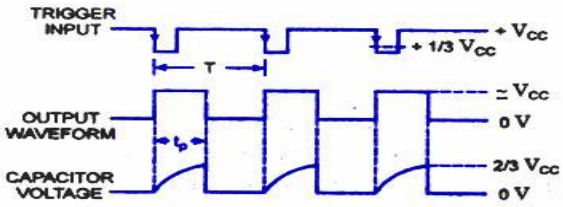
Circuit of The Timer 555 as a Monostable Multivibrator

OPERATION:

Let consider the output of the flip flop is low then he circuit is in stable state. If we are giving negative pulse to the comparator2 means the output of the comparator goes high when the trigger voltage falls to 1/3Vcc and it will reset the flip flop. So the transistor goes to off state, then the output of the flip flop goes high. This is called the transition of the output from stable to quasi-stable state, as shown in figure.



Internal Circuitry With External Connections



Trigger Input, Output and Capacitor Voltage Waveforms

Monostable Operation

As the discharge transistor is cutoff, the capacitor C begins charging toward $+V_{CC}$ through resistance R_A with a time constant equal to R_AC. When the increasing capacitor voltage becomes slightly greater than +2/3 V_{CC}, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low.

the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

tp = 1.0986 R_AC

vc = VCC (1- e-t/R_AC)

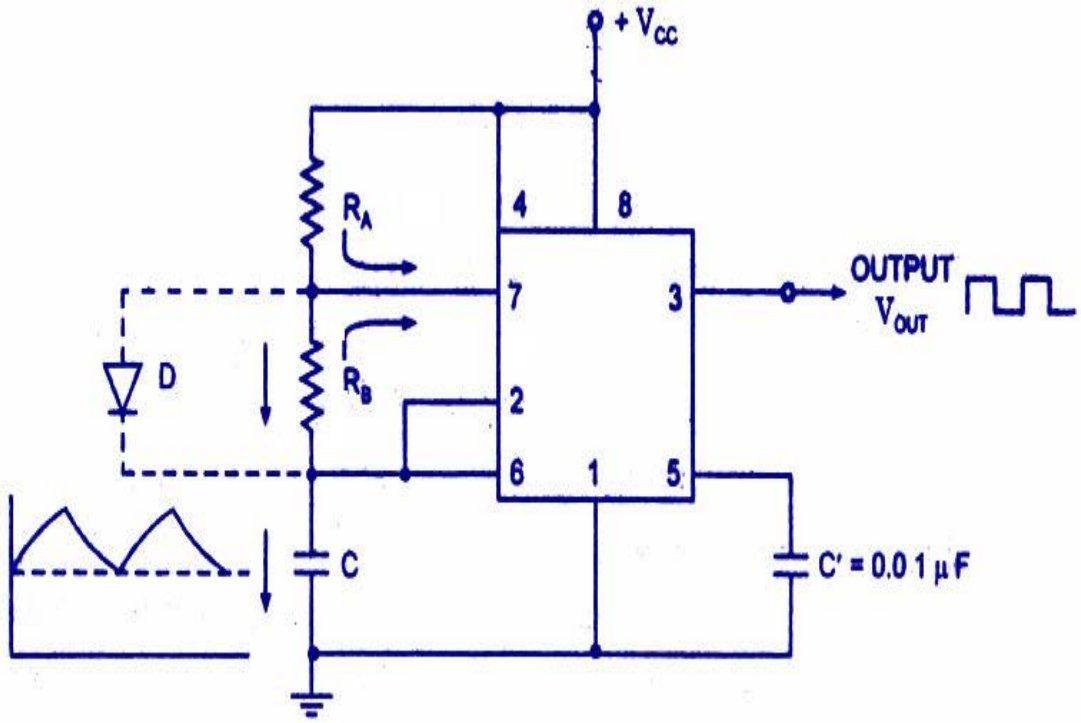
Substituting **vc = 2/3 VCC**

So **+2/3VCC. = VCC. (1 – e–t/R_AC) or t – R_AC loge 3 = 1.0986 R_AC**

So pulse width, **tP = 1.0986 R_AC s 1.1 R_AC.**

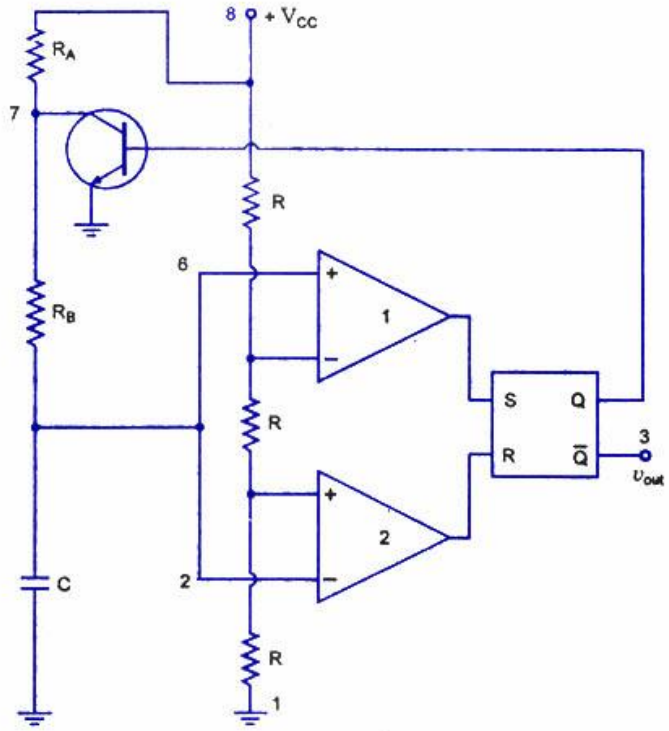
ASTABLE MULTIVIBRATOR

An astable multivibrator is also called as free running multivibrator In astable multivibrator there is no need of providing trigger to change its states hence the name free running multivibrator.

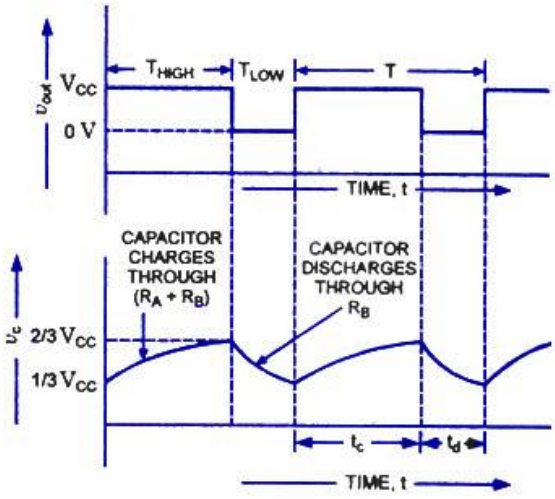


Circuit of The Timer 555 as an Astable Multivibrator

For explaining the operation of the **timer 555** as an astable multivibrator, necessary internal circuitry with external connections are shown in figure.



Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

Astable Operation

Astable-Multivibrator-Operation

Initially consider the output Q is in low state ,then the transistor is goes to off state and capacitor get charge by Vcc through the voltage divider network R_A and R_B.

Then the charging time can be written as

$T= (R_A + R_B)C$

If the threshold voltage of comparator1 is exceeds means then the comparator produces high output and the output of comparator1 makes the flip flop to set state and also it leads to produce the output of flip flop Q to high. So the timer output is low since the timer output is depends on $\overline{Q}$ .The capacitor discharges and its time constant becomes R_BC. Now the voltage of comparator 2 is decreased, and if it is decreased to 1/3Vcc then the output of comparator is high it leads to reset the flip flop. The output of the timer becomes high. Thus it is a continuous process.

t_c or THIGH = 0.693 (R_A + R_B) C

Voltage across the capacitor is given as, **v_c=VCC(1-et/RC)**

The time taken by the capacitor to charge from 0 to +1/3 V_{CC}

1/3 VCC = VCC (1-et/RC)

The time taken by the capacitor to charge from 0 to +2/3 V_{CC}

t2 = RC loge 3 = 1.0986 RC

So the time taken by the capacitor to charge from +1/3 V_{CC} to +2/3 V_{CC}

tc = (t2 – t1) = (10986 – 0.405) RC = 0.693 RC

Substituting R = (R_A + R_B) in above equation we have

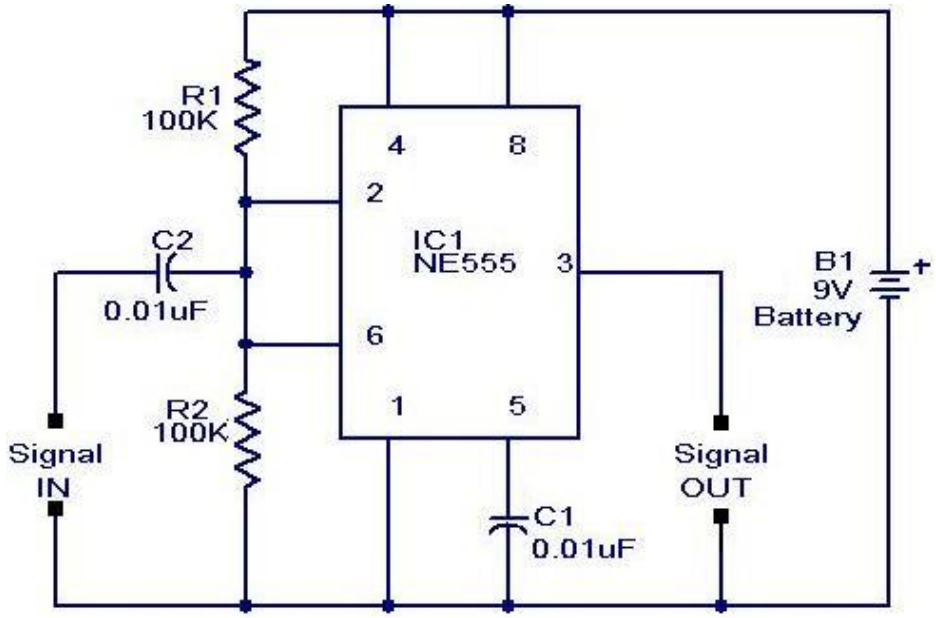
T_{HIGH} = tc = 0.693 (R_A + R_B) C

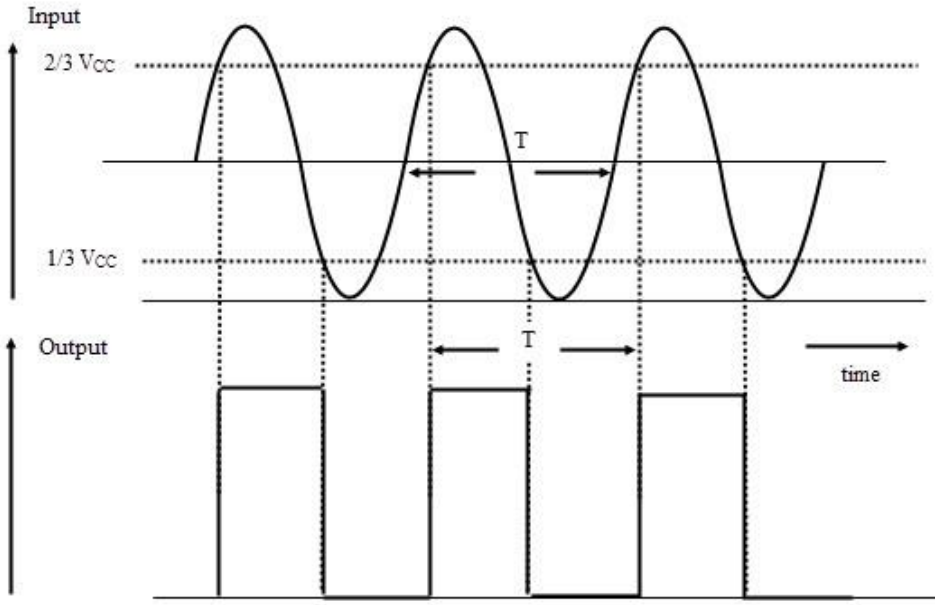
where R_A and R_B are in ohms and C is in farads.

SCHMITT TRIGGER

Circuit of 555 timer as Schmitt Trigger

The following circuit shows the structure of a 555 timer used as a Schmitt trigger.





In the above diagram, resistors R1 and R2 act as a voltage divider and the divider circuit provides the voltage Vcc/2 to the capacitor to it. Internally the circuit has 2 comparators .Comparator1 operates at 2/3 Vcc and the lower comparator operates 1/3 Vcc. These two comparator's output is connected with the flip flop and these comparator output only can decide the state of the flip flop i.e. to set or reset. The output of the Schmitt trigger is high when input voltage is higher than the upper threshold 2/3Vcc. The output of the Schmitt trigger is low when input voltage is lower than the lower threshold 1/3Vcc .

The usage of two threshold values is called Hysteresis and the Schmitt trigger acts as a memory element (a bistable multivibrator or a flip-flop).

Voltage regulator

It is a 3 pin IC. The main purpose of voltage regulator is to provide constant output. The output of the voltage regulator is remains constant irrespective of the change in input or change in load.

Types:

Types of IC voltage regulators

There are basically 4 types.

1. Fixed positive voltage regulator

2. Fixed negative voltage regulator

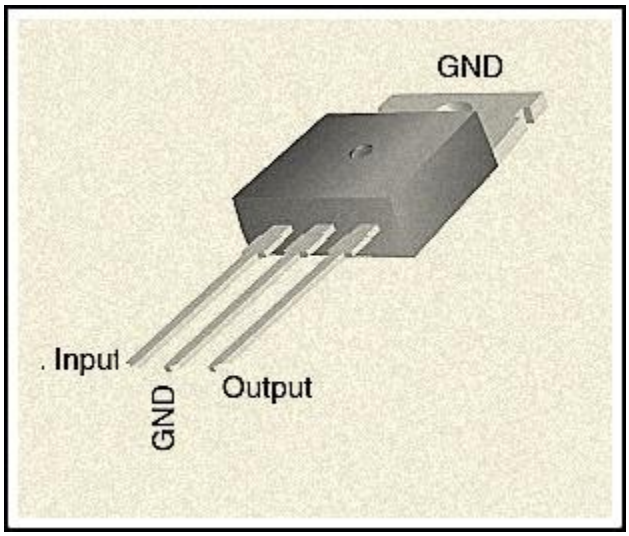
3. High voltage and low voltage regulator

4. Adjustable voltage regulator

5. Dual tracking voltage regulator

1. Fixed Positive voltage regulator

Pin diagram:



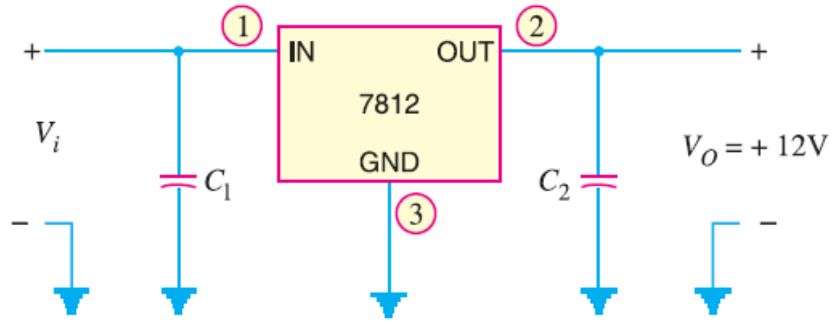
It is a 3 pin voltage regulator IC.

Pin 1: Input pin

Pin 2: Ground

Pin 3: output

Circuit diagram:

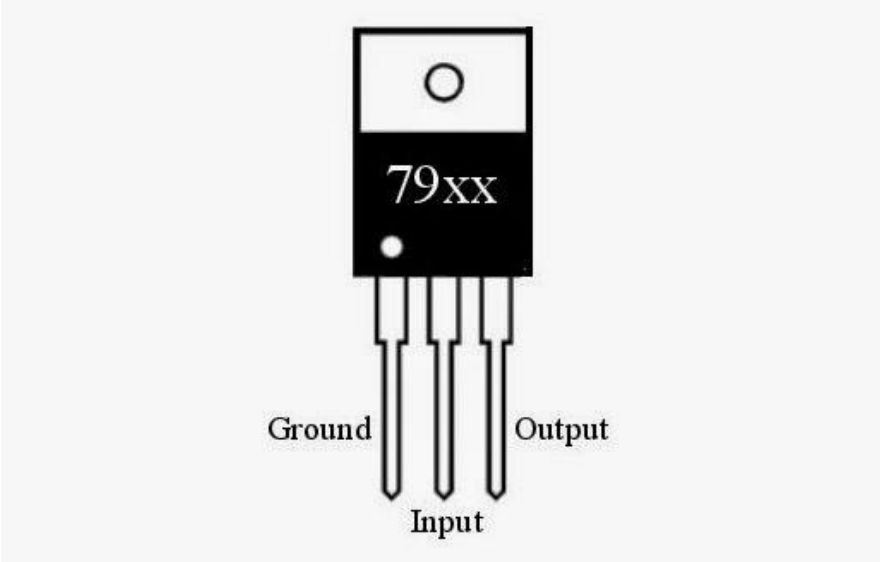


As per the pin diagram in the above circuit diagram input voltage is given to the pin-1, the output is taken from the pin-2 and the pin-3 is grounded. The positive voltage regulator provides positive voltage at its output. The best example for positive voltage regulator is 78xx IC. The last two digits or symbol 'xx' represent a level of voltage the can be produced at its output. For an example 7805 IC regulator provides constantly +5V at its output.

The types of ICs and its voltage ranges are given in the following table.

IC No	Voltage
7805	5V
7806	6V
7808	8V
7809	9V
7810	10V
7812	12V
7815	15V
7818	18V
7824	24V

2. Fixed Negative voltage regulator



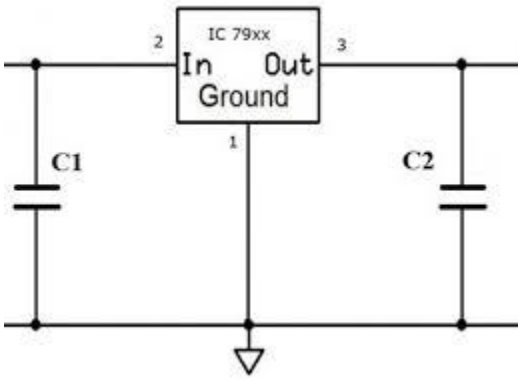
It is a 3 pin voltage regulator IC.

Pin 1: Ground

Pin 2: Input pin

Pin 3: output

Circuit dagram:



As per the pin diagram, in the above circuit diagram input voltage is given to the pin-2, the output is taken from the pin-3 and the pin-1 is grounded. The

negative voltage regulator is same as the positive voltage regulator but the negative voltage regulator provides negative voltage at its output. The best example for negative voltage regulator is 79xx IC. The last two digits or symbol 'xx' represent the voltage level, for an example 7905 Ic regulator provides constantly -5V at its output.

The types of ICs and its voltage ranges are given in the following table.

Type number	Output voltage
7905	−5.0 V
7905.2	−5.2 V
7906	−6.0 V
7908	−8.0 V
7912	−12.0 V
7915	−15.0 V
7918	−18.0 V
7924	−24.0 V

The 7900 series

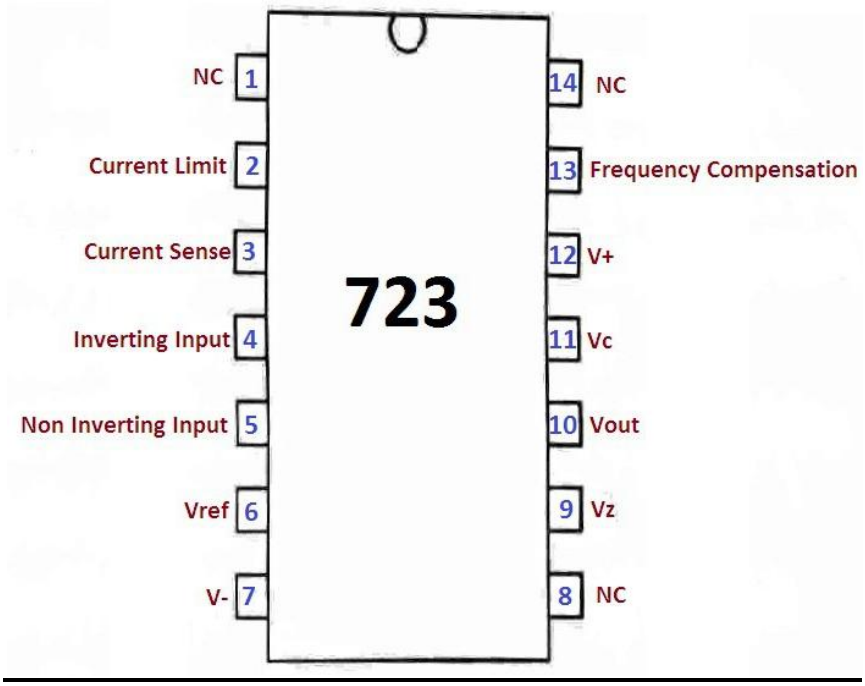
The positive and negative voltage is commonly called as fixed voltage regulators.

B. Based on voltage level:

High voltage and low voltage regulator

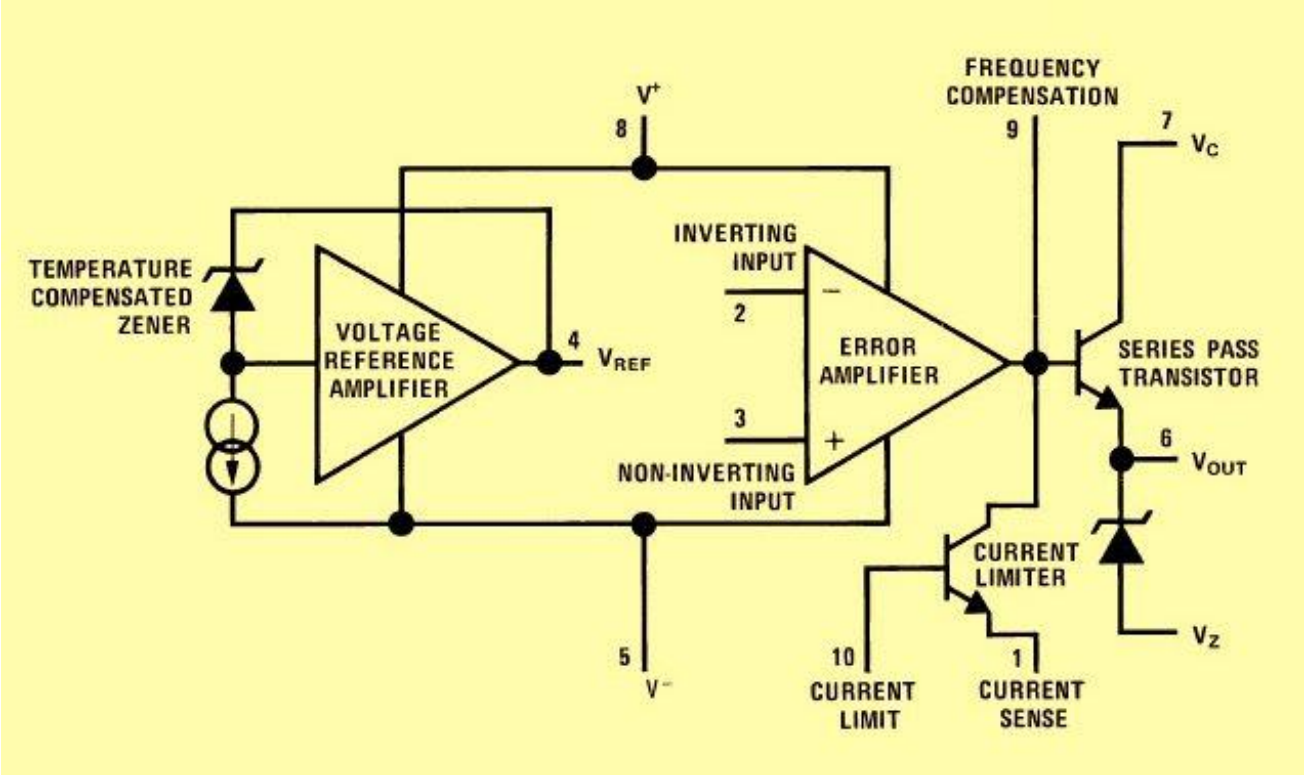
GENERAL PURPOSE REGULATOR USING LM 723

PINDIAGRAM



It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both positive and negative voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

Internal Block Diagram



723 Voltage Regulators Internal Block Diagram

The internal working can be explained by dividing it into two blocks, **the reference voltage generator** and **the error amplifier**. In the reference voltage generator, a zener diode is being compelled to operate at fixed point (so that zener output voltage is a fixed voltage) by a constant current Source which comes along with an amplifier to generate a constant voltage of 7.15V at the Vref pin of the IC.

As for the error amplifier section, it consists of an error amplifier, a series pass transistor Q1 and a current limiting transistor. The error amplifier can be used to compare the output voltage applied at Inverting input terminal through a feedback to the reference voltage Vref applied at the Non-Inverting input terminal. These connections are not provided internally and so have to be externally provided in accordance with the required output voltage. The conduction of the transistor Q1 is controlled by the error signal. It is this transistor that controls the output voltage.